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Investigation of Superlattice Device Structures

**Isoris S. Gergis, Harold M. Manasevit,
Alice L. Lin, and A. Brooke Jones**

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SECTION I

INTRODUCTION

The purpose of this program was to explore superlattice structures (i.e. ultrathin periodically layered semiconductor heterostructures) in silicon-based semiconductors and to explore the device applications in such structures.

Research in superlattice structures in III-V compound semiconductors (Ref 1, 2) resulted in the discovery of new phenomena such as negative differential conductivity normal to the superlattice axis and enhanced electron mobility (Ref 2) due to the formation of a 2-dimensional electron gas at the heterojunctions in the superlattice. While the former was a direct result of coherent scattering of electrons by the superlattice potential, the latter phenomenon is in fact a heterojunction phenomenon and occurs even in a single selectively doped heterojunction between two semiconductors with specific band structure line-up and doping profile (Ref 3).

Mobility enhancement was observed in MOS electron inversion layers as a result of the splitting of the conduction band minima in the narrow energy well created by the application of the gate voltage (Ref 4). Si-based superlattice structures (Ref 5) specifically Si/Si_{1-x}Ge_x, were also predicted to exhibit electron mobility enhancement due to basically the same mechanism - this time by the perturbation due to the superlattice potential.

Several schemes (Ref 6) have been proposed for the realization of superlattice structures in silicon by means of lithographic techniques. Another means of constructing a periodic structure is the now familiar technique of epitaxial deposition of semiconductor thin films of different composition but with small lattice mismatch. After reviewing the lithographic resolution requirements for superlattice structures where the electron mean free path ($\sim 300\text{\AA}$) is comparable to the superlattice period, we decided to pursue the second approach of epitaxial growth of thin alternate layers of Si and Si_{1-x}Ge_x. The value of x was to be determined experimentally as evidenced by the crystalline quality of the multilayer films. The method of deposition was chemical vapor deposition (CVD) by the pyrolysis of SiH₄ in an H₂ atmosphere. The choice of the deposition technique was dictated by the availability of a Silicon CVD System in our laboratories at MRDC. Although the molecular beam epitaxy (MBE) technique offers much better control of the layer thickness, we thought the CVD technique should provide sufficient thickness control for fabricating the superlattice structure. In fact, films with individual layer thickness of about 300 \AA had clear layered structure as seen with scanning electron microscopy (SEM) and Auger electron spectroscopy (AES) depth profiling.

The program evolved into several phases: the first phase was one of exploratory nature in which films with different parameters were grown and evaluated. The parameters that were varied were layer composition (percentage Ge in the alloy layers), individual layer thickness, number of layers, and growth temperature. The evaluation of the films consisted of measuring the conductivity, carrier concentration, and mobility (Hall effect) at room temperature and 77°K, and examination of the film cross section by SEM. The film composition was determined using energy dispersive X-ray spectroscopy (EDXS) to measure the average film composition. Auger profiling and secondary ion mass spectroscopy analyses were made for several films to determine the compositional profile of the layered structure. During that phase we found that the Hall mobilities measured in multilayer films whose parameters are within a certain range were consistently higher (sometimes by a factor of 50 percent) than those of single layer Si or SiGe films of comparable thickness and carrier concentration.

This finding led to the second phase of the program where systematic study of the effect of the film growth conditions on the film properties was made. The growth conditions that were studied were the doping concentration, growth temperature, substrate orientation and the Ge content in the alloy layers. A fairly large number of films were fabricated and evaluated. In parallel with these activities, physical characterization of the films was performed in an effort to explain the observed mobility enhancement in terms of the film structure. The film electrical parameters were measured from room temperature down to 20°K. X-ray double crystal diffraction rocking technique was used to measure the elastic strain, the strain relief, and the unstrained lattice constants of the layers of the films. Transmission electron microscopy (TEM) examinations of some films were made.

The third and last phase of the program was to fabricate MESFET and MOSFET devices on suitable multilayer films for integrated circuit applications and to use the devices to measure the local electrical properties of the film as a function of depth.

The results obtained from the analytic investigation shed considerable light on the cause of the observed enhanced electron mobility in these films and revealed very interesting features of their electronic structure. The results show electron confinement at the alternate interfaces of the Si and SiGe layers, namely, the interfaces with the SiGe on top of Si. The cause of this confinement is not yet clear although it might be due to the conduction band discontinuity at the heterojunction. The confinement then results in the splitting of the energy band minima of the conduction band as described by Moriarty and Krishnamurthy (Ref. 5) The resulting redistribution of electrons among the sub-bands leads to enhanced mobility for sufficiently low electron density and large enough band splitting compared to the thermal energy kT . This can account for the observed 40-50 percent mobility enhancement observed in these films.

This report is divided into six sections with the first being this introduction. Section II details the film growth conditions and their effects on the film electrical parameters. Section III describes the investigation of the film structure by various analytic techniques. Section IV describes the experiments and results of the characterization of the electrical properties of the film including those obtained from the field effect transistors. Section V describes the device fabrication processes and Section VI contains discussion and conclusions.

The authors would like to acknowledge the contributions by Howard Glass (x-ray double crystal diffraction experiment), Jane Yang (Hall measurements), and Ilan Golecki (RBS measurements) and the skilled assistance of Sigfried Plonski, Jane Cooper, Roy Harada, Nancy Casey, and Carol Sallee in device fabrication.

SECTION II

CVD GROWTH OF THE MULTILAYER Si/Si_{1-x}Ge_x FILMS

This section describes the film growth technique using chemical vapor deposition (CVD) and the effect of the film growth conditions on the film properties. We will discuss the properties in terms of carrier mobility, carrier concentration, Ge content, and film appearance. The Van der Pauw method was used to determine the resistivity and Hall coefficient from which the carrier concentration (n) and mobility μ were deduced. The Ge content was determined by Energy Dispersive X-ray Spectroscopy (EDXS) and AES. The film thickness, which in turn determines the superlattice period, was measured using the SEM. Visual observation of the films during and after growth gave indication of the film quality.

The CVD growth of the films employed hydrides as sources of Si and Ge. CVD growth of SiGe alloys on Si using the halides was reported as early as 1962 by Oda (Ref 7) and Miller and Grieco (Ref 8) and in 1972 by Aharoni and co-workers (Ref 9), but films from the halides require high growth temperatures (1100-1200°C) (Ref 9,10), and layer dopant interdiffusion would be expected at these temperatures. In addition, the generated HCl would also be expected to cause problems in composition and doping control of very thin layers due to a competing film-growth and etch-back process. On the other hand, epitaxial SiGe layers have been grown from the hydrides on Ge as low as 800°C (Ref 11) and on Si as low as 1000°C (Ref 12). We prepared Si and SiGe alloy layers and films from one SiH₄ source (5 percent in He) and two GeH₄ sources (5.5 percent in H₂ and 5.5 percent in He) in a Pd-purified H₂ carrier gas on high resistivity single crystal p-type Si substrates. Intentionally added dopant species were from proportioned flows of phosphine (PH₃, 45ppm in He) and diborane (B₂H₆, 46ppm in He). Total gas flow was about 3 lpm.

Apparatus

The films were grown in a CVD reactor system, a schematic of which is shown in Figure 1. It consists essentially of: (1) a reactant gas manifold and distribution line system of mostly 1/4 in. valving, filters and flow controls, (2) a vacuum pumping system for evacuating selected portions of the reactor system as needed, (3) provisions for burning the reactor exhaust gases, and (4) a 75mm diameter vertical quartz deposition chamber with provision for supporting the substrates normal to gas flow on a rotatable SiC-coated graphite susceptor. The susceptor is inductively heated by a radio frequency coil that surrounds the deposition chamber. An automatic sequence timer with a mechanical counter in series is used to control solenoid-activated air-operated valves for rapid and precise flow control of the gases and reactants. Doping gases were injected into the SiH₄ line. A separate line was used for the GeH₄, with both lines joining near the top of the deposition chamber. Temperatures were measured with an optical pyrometer that was focused on the side of the rf-heated susceptor. The actual temperature at the top of the susceptor is lower than the reported measured temperature by about 50°C when the side-temperature is about 1000°C.

In the following we describe the experiments performed for investigating the effects of the growth conditions on the films properties.

Growth Temperature Studies

The initial phase of the experiments determined the minimum temperature at which reasonable quality single-layer films of Si and SiGe could be grown in our system on (100)-oriented Si substrates. The temperature range 900-1000°C was examined; and based on the reflectivity and

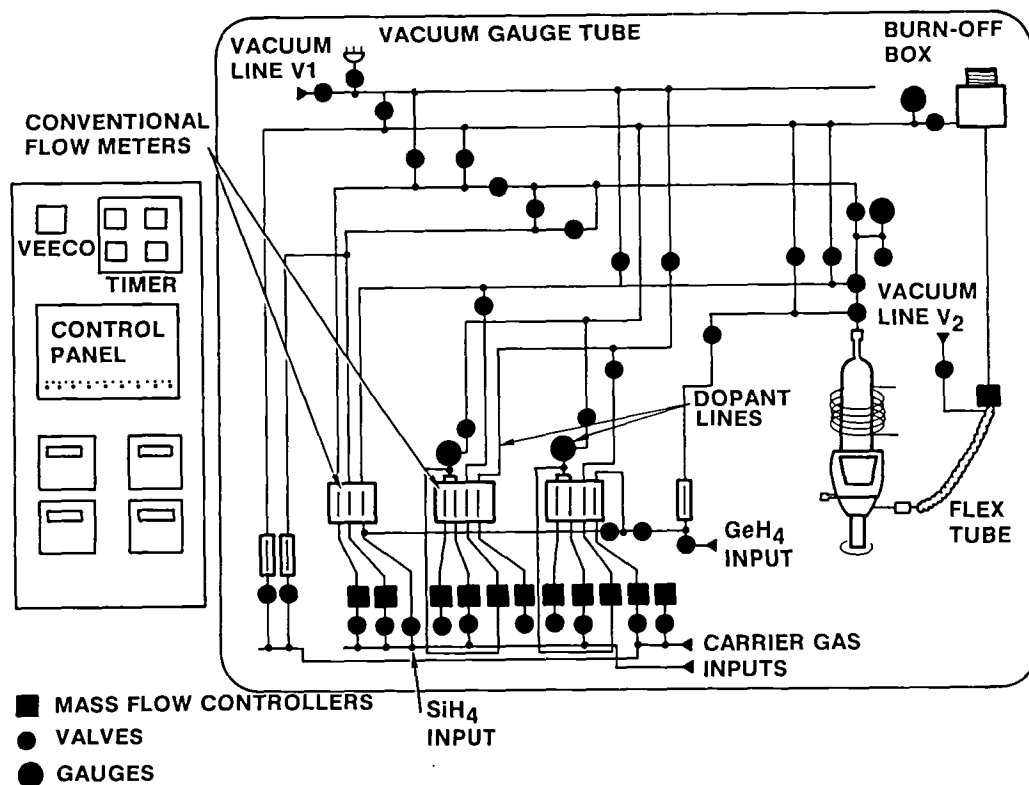


Figure 1. Schematic Diagram of the Si CVD Reactor System

smoothness of these (100)-oriented films, 1000°C was established as a preferred growth temperature. As shown in Figure 2, during these early experiments it was found that the incorporation of Ge into the film was temperature dependent, i.e., more Ge was incorporated in the film at 900°C than at 1000°C for the same reactant gas flow rates. The wall deposit was heavy where SiH₄-GeH₄ mixtures were pyrolyzed, and the growth rate was mainly influenced by the SiH₄ flow at a growth temperature of ~1000°C. Si films were high resistivity, and SiGe films were n-type (~10¹⁶cm⁻³) at growth rates of ~0.3μm/min. At this growth rate and temperature the Ge mole fraction was ~0.08-0.10. By lowering the SiH₄ flow (from a value of 50 to 10ccpm), the films became p-type for rates of ~0.1μm/min. using the original tanks of SiH₄ and GeH₄. The films became more p-type as the Ge content increased (up to at least 9.27 mole fraction Ge), thereby necessitating the addition of an n-type dopant, phosphorus, to produce n-type films.

When a second tank of GeH₄ (~5 percent in He) was used in combination with the same tank of SiH₄, the "undoped" SiGe films were n-type. It was also determined that single films of Si were now n-type with $n \sim 1-2 \times 10^{15} \text{cm}^{-3}$ rather than high resistivity, as previously found. A series of multilayer growth experiments which repeated many of those performed with the first GeH₄ tank, but without PH₃ additions, led to similar electrical results.

Table 1 compares the properties of phosphorus-doped single layer Si and SiGe films and multilayered Si/SiGe films grown at the higher rate at three different temperatures. We note that the thicker ~10 mole percent Ge films grown even as low as 900°C show comparatively high mobilities (~1350cm²/V-sec for $n \sim 10^{16} \text{cm}^{-3}$) even though the films are probably compensated. During the early stages of growth the films were gray, but they slowly changed in reflectivity as

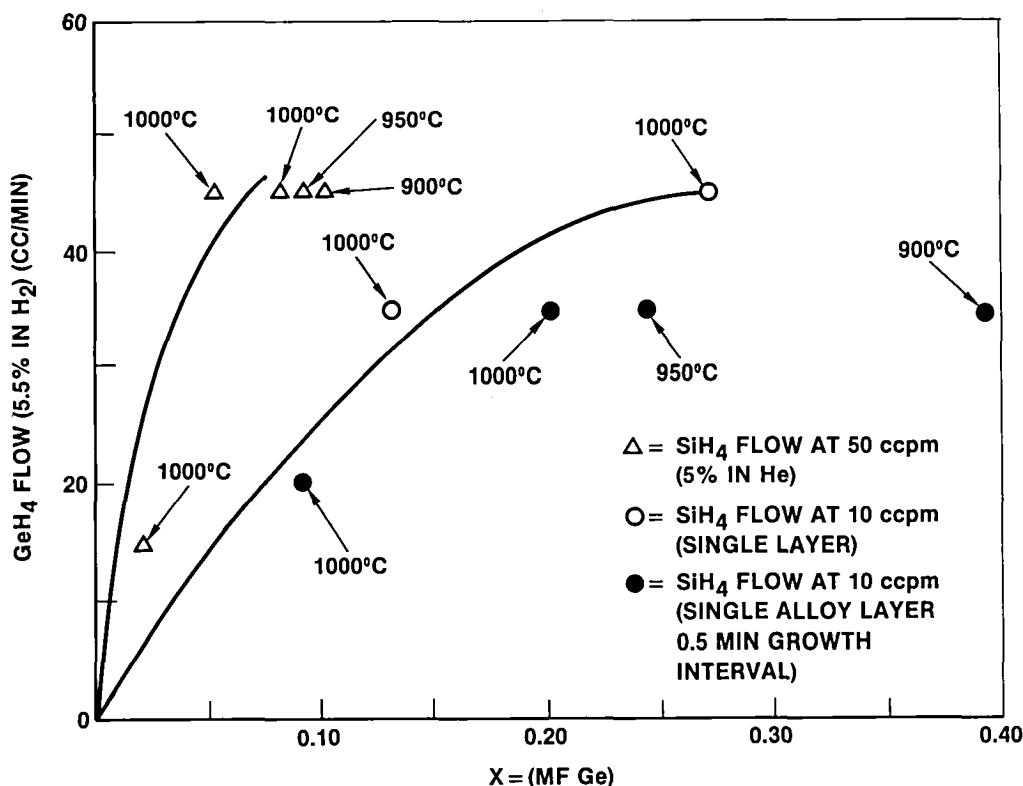


Figure 2. Effect of GeH_4 Flow and Growth Temperature on the Film Composition of $\text{Si}_{1-X}\text{Ge}_X$ Alloy Layer

Table 1. Characteristics of Si: P, SiGe: P, and Si: P/SiGe: P Films Annealed for 0.5 Min Between Layers

SEQ. NO.	GROWTH TEMP (°C)	FLOWS (ccpm)* SiH_4 - GeH_4	GROWTH TIME (MIN)	TOTAL NO. OF LAYERS	APPROX. THICKNESS μm A/LAYER		M.F. Ge (EDAX)	RESIST (ohm-cm)	ELECTRON CONC. (cm^{-3})	ROOM TEMP. MOBILITY ($\text{cm}^2/\text{V-sec}$)
15	~1000	50-0	25	1	8	-	-	0.23	3.5×10^{16}	784
16	~1000	50-45	25	1	9	-	0.08	0.52	1.9×10^{16}	620
17	~1000	$\begin{cases} 50-0 \\ 50-45 \end{cases}$	$\begin{cases} 0.2 \\ 0.2 \end{cases}$	20	1.2	600	-	1.1	1.7×10^{16}	347
23	~950	50-0	50	1	9	-	-	0.47	2.3×10^{16}	569
24	~950	50-45	25	1	10	-	0.09	0.27	5.2×10^{16}	442
20	~950	$\begin{cases} 50-0 \\ 50-45 \end{cases}$	$\begin{cases} 0.2 \\ 0.2 \end{cases}$	100	5.2	520	-	0.43	1.1×10^{16}	1330
11	~900	50-45	25	1	10	-	~0.10	0.17	1.3×10^{17}	276 (p-type)
21	~900	$\begin{cases} 50-0 \\ 50-45 \end{cases}$	$\begin{cases} 0.4 \\ 0.2 \end{cases}$	100	6.6	660	-	0.26	1.6×10^{16}	1469
39	~900	$\begin{cases} 50-0 \\ 50-45 \end{cases}$	$\begin{cases} 0.1 \\ 0.1 \end{cases}$	100	3.2	320	-	0.52	8.8×10^{15}	1370

they became thicker, ending as semi-reflective films. The thickness of each Si and SiGe layer was controlled by injecting the reactants into the deposition chamber for a specified time period. In the study, 0.5 min. was arbitrarily used between layer growths to purge the lines and reactor of residual dopants and reactants. Thus, the 100-layer structure shown in Figure 3 was produced at 950°C by 0.2 minute bursts of the silane source at 50ccpm and 0.2 minute bursts of the combined SiH_4 and GeH_4 sources, the latter at 45ccpm.

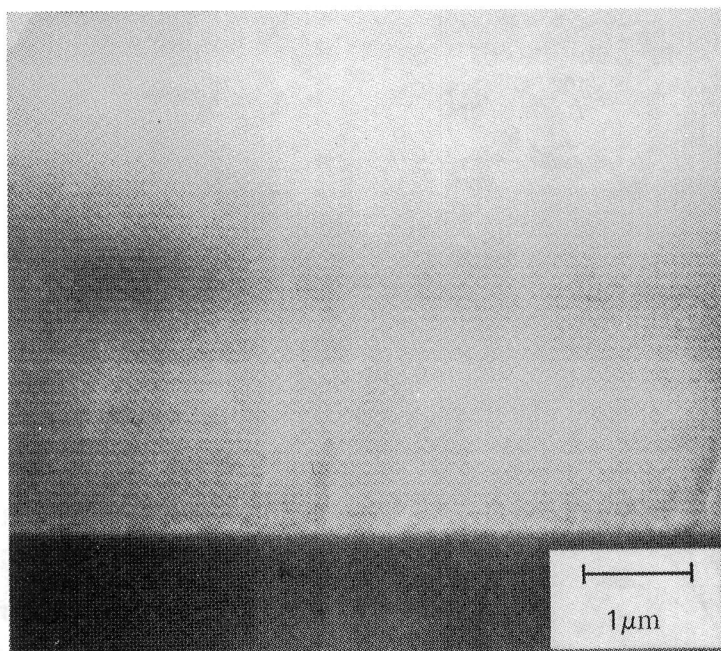


Figure 3. SEM Photograph of A 100 Layer Alternating Multilayer Si/Si_{0.85}Ge_{0.15} Film, $\sim 5 \mu\text{m}$ Thick. The Individual Si and SiGe Layers are $\sim 500 \text{ \AA}$ Thick as Determined by an Auger Profile.

Layer Thickness Dependence

The room temperature mobilities of thick multilayer Si/SiGe films grown at $\sim 1000^\circ\text{C}$ at the lower growth rate ($\sim 0.1 \mu\text{m}/\text{min}$) using both GeH_4 cylinders for Si_{1-x}Ge_x layer compositions of $x = 0.10$ and $x = 0.15$ are shown in Figure 4 as a function of the Si layer thickness. In all cases, the thickness of the SiGe layer was either equal to or greater than that of the Si layer. The doping levels in the SiGe films are $\sim 10^{15} \text{ cm}^{-3}$; in the Si, $\sim 10^{15} - 10^{16} \text{ cm}^{-3}$. The data indicate higher mobilities in the layered Si/SiGe films with 15 mole percent Ge in the SiGe layers for a Si layer thickness of $\geq 400 \text{ \AA}$. Good mobilities ($\sim 1000 \text{ cm}^2/\text{V}\cdot\text{sec}$) were found for multilayer films with Si layer thicknesses as thin as 250 \AA .

In Figure 4, in the sequences 29, 53 and 54, the Si layer thickness was kept constant at $\sim 400 \text{ \AA}$ and the SiGe layer thickness was progressively increased from $\sim 400 \text{ \AA}$ to $\sim 1500 \text{ \AA}$. The results (< 10 percent mobility difference) indicate the thickness of the SiGe layer has little effect on the electrical properties of film grown under these conditions of temperature, growth rate, layer composition, etc.

Comparatively poor electrical results were obtained for layers grown with an injection time of 0.2 min ($\sim 200 \text{ \AA}$ layer thickness). This may be due to a combination of insufficient gas mixing in the reactor and layer inter-diffusion, for even the SEM at high magnification was unable to reveal a layered pattern in such films.

Film Thickness Dependence

The electrical properties of the alternating Si/SiGe multilayer films were found to be dependent on the total film thickness for films $\leq 2 \mu\text{m}$ thick. The results in Figure 5 include data for two dif-

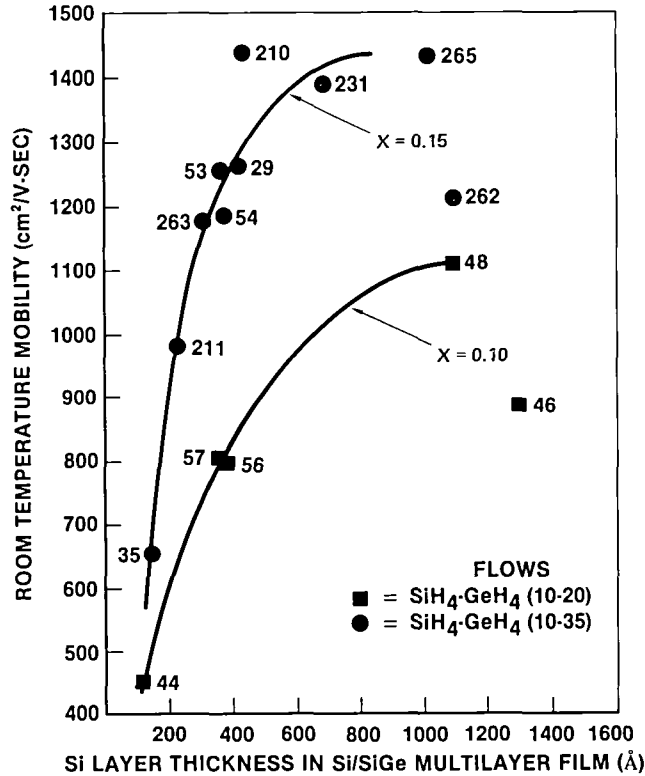


Figure 4. Mobility Versus Si Layer Thickness in Si/Si_{1-X}Ge_X Multilayer Films with X = 0.1 and 0.15. Layer Growth Rates Were ~ 0.1 Per/Min at a Growth Temperature of ~ 1000°C. Measured Carrier Concentrations were from 8×10^{15} to 3×10^{16} cm⁻³. Total Film Thickness was between 2 μ m and 6 μ m.

ferent sets of films: one in which the Si layers are about 500Å thick and the SiGe layers ~1000Å thick; and the other for films grown with layers of different thickness produced using the same injection times for the Si and SiGe layer in each film (from 0.3 min. to 1.5 min.).

The main feature observed in Figure 6 is that the electron mobility decreases steadily for film thickness smaller than 1 μ m or thereabout. As will be discussed later, this is most likely due to the unevenness in the growth of the first few layers of the film. This was observed in the TEM examination of the films and was also confirmed in the profiling of the electrical properties of the films.

Substrate Orientation Effect

Films were grown on (111) oriented substrates with film thickness about 0.25, 2.0 and 4.0 μ m. The growth conditions were similar to those on (100) substrates. Table 2 provides a comparison between the electrical parameters of those films to films grown on (100) substrates. The electron mobility in the (111) films is consistently smaller than the mobility in (100) films by a factor of 2 or more. This result, as will be discussed later, is consistent with the proposed mechanism of mobility enhancement which predicts that the enhancement should occur in the (100) and not in the (111) oriented films.

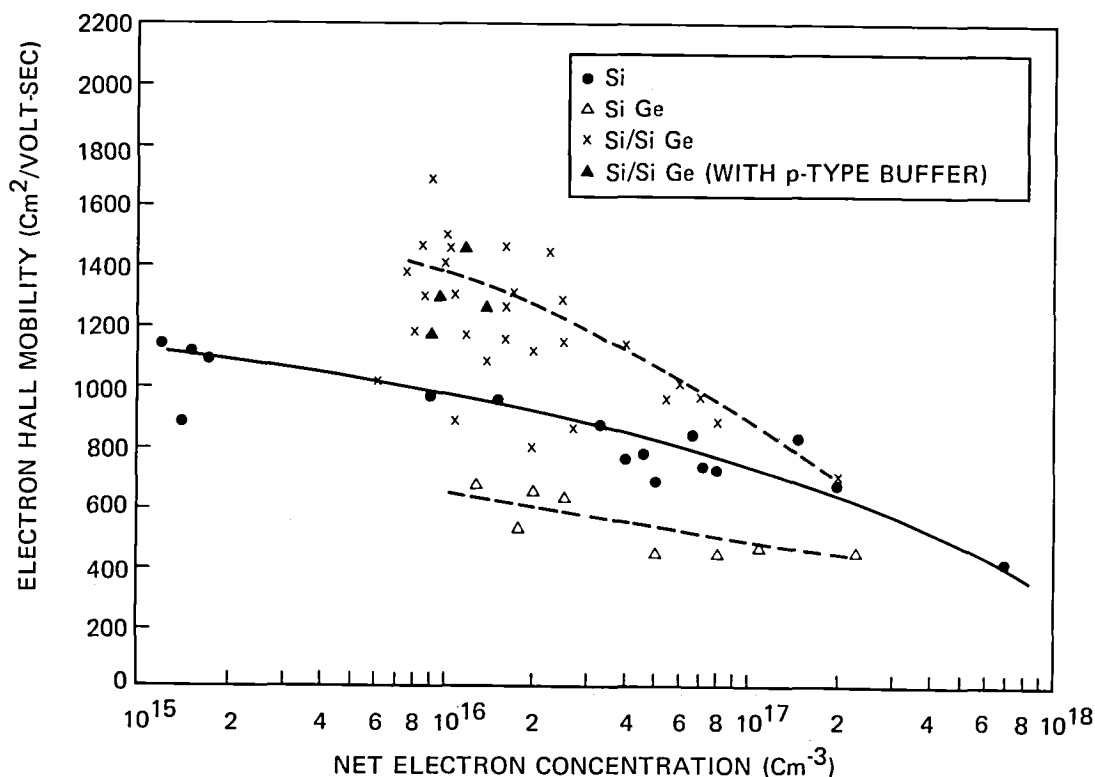


Figure 5. Electron Hall Mobility vs Net Carrier Concentration for (100)-Oriented Si (●), Si_{1-x}Ge_x(Δ), and Alternating Layer Si/SiGe (X, ▲) Films Grown Under Somewhat Similar Conditions for X Between 0.10 and 0.22 for Film Thickness Between 2.0 and 6.5μm, and Si/SiGe Layer Thickness Between 300Å and 1500Å.

Carrier Concentration Dependence

To determine the properties of films of Si, SiGe, and multilayered Si/SiGe (100)-oriented films of different electron concentration levels, a PH₃-He source was proportioned and mixed with the SiH₄ and SiH₄-GeH₄ mixtures just prior to film growth. The electrical results are summarized in Figure 5 along with data from many other films grown during the course of the study.

The results show a mobility enhancement of from ~20 percent to at least 40 percent in the multilayer Si/SiGe films over that of epitaxial Si layers and ~100 percent over that of epitaxial SiGe layers for n from ~8x10¹⁵ to ~10¹⁷cm⁻³.

Limited studies gave no indication that hole mobilities are enhanced in Si:B/SiGe:B multilayers. On the other hand, low mobility values may be due to the fact that the B-doped p-type films are compensated by the n-type impurities present in the source gases.

Annealing Effects

Experiments were made to explore the effect of extended annealing in H₂ on film properties. The electrical parameters were first measured before annealing and a second time after annealing. The annealing was performed at 1000°C for 2 hr in H₂ atmosphere. This extended annealing resulted in no change or a slight decrease in the electron mobility.

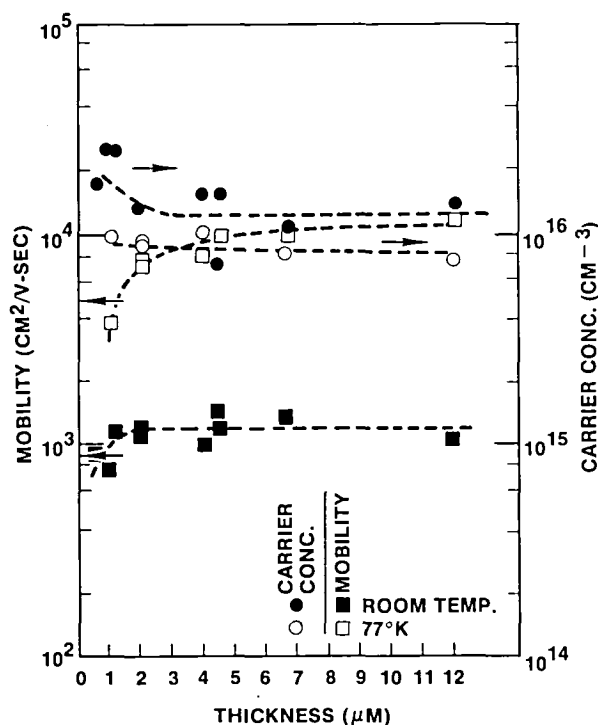


Figure 6. Carrier Concentration and Mobility Versus Thickness for Undoped Multilayer Si/Si Ge Films

Table 2. Effects of Substrate Orientation on Film Properties (Growth Temperature ~ 1000°C)

SEQ. NO.	SUBSTRATE ORIENT.	FLows (ccpm) SiH ₄ -GeH ₄	GROWTH TIME (MIN)	TOTAL NO. OF LAYERS	APPROX. THICK (μm)	RESIST. (ohm-cm)	CARRIER CONC. (cm ⁻³)	MOBILITY (cm ² /V-sec)
115	100 } 111 }	10 - 35	2.3	1	0.25	0.30 0.50	8.3 × 10 ¹⁶ 3.3 × 10 ¹⁶	252 376
114								
	100 } 111 }	10 - 35	20	1	2	1.0 0.6	1.5 × 10 ¹⁶ 2.4 × 10 ¹⁶	406 474
269	100 } 111 }	10 - 0 10 - 35	0.6	61	4.5	0.36 0.08	1.5 × 10 ¹⁶ 7.9 × 10 ¹⁵	1185 9462
			0.6					
		10 - 0 10 - 35	0.6	61	4.5	0.86 0.33	1.0 × 10 ¹⁶ 5.6 × 10 ¹⁵	719 3357
			0.6					

Buffer Layer Experiment

As mentioned earlier, multilayer films with total thickness less than 1.0 μm showed lower mobilities than thicker films. This observation raised the possibility that there might be problems associated with growing directly on the substrate surface. Experiments were made to determine the properties of thin films grown on a buffer layer of Si and/or SiGe. To this end, flow conditions were sought using B₂H₆ in He to produce a P-type buffer layer that would just compensate the n-type impurity in the Si and SiGe layers. P-type alloy films were grown with net hole concentra-

tions of $\sim 10^{16} \text{cm}^{-3}$ and resistivities as high as $4 \Omega \text{cm}$. Alternate P-type multilayer buffer Si/SiGe structures were then grown followed by thin n-type alternating Si/SiGe structures. Several films of about $1.0 \mu\text{m}$ thickness showed electron mobility up to $\sim 1100 \text{ cm}^2/\text{volt}\cdot\text{sec}$ compared to 800 to $900 \text{ cm}^2/\text{volt}\cdot\text{sec}$ for films grown directly on the Si substrates. Buffer layers of single layer p-Si and multilayer Si/SiGe (also p-type) showed similar results. Thus, it appears that the buffer layer improves the multilayer film quality as reflected in higher carrier mobility.

Summary

Enhanced electron mobility was found in n-type multilayer films under the following conditions:

1. Layer thickness between 300\AA to 1500\AA .
2. Total film thickness $> 1.0 \mu\text{m}$.
3. Growth temperatures between 950°C and 1025°C with a few good films grown at about 900°C .
4. Alloy layer composition of 10 to 20 percent Ge.
5. Dopant concentration (or more accurately the average carrier concentration) from 7×10^{15} to $2 \times 10^{17} \text{cm}^{-3}$.
6. Substrate orientation (100), but not (111).

SECTION III

INVESTIGATION OF THE FILM STRUCTURE

In this section we describe the experiments performed to determine the physical structure of the multilayer films. Rutherford backscattering (RBS), Auger electron spectroscopy (AES), and secondary ion mass spectroscopy (SIMS) were used to determine the Ge depth profile in the films. Energy Dispersive X-ray Spectroscopy (EDXS) provided the average percent Ge in the film. X-ray double crystal rocking technique was used to determine the lattice constant, elastic strain, and strain relief in the Si and SiGe layers. Transmission electron microscopy (TEM) was used to examine the crystalline quality of the film and its interface with the substrate. Scanning electron microscopy was used routinely to examine the film cross sections and in some cases the surface of the films and provided an accurate measurement of the film thickness and hence, the periodicity of the superlattice.

Germanium Depth Profile

Some of the early films were analyzed by RBS which provided a quantitative measurement of the Ge percent in the film and its profile with depth. Figure 7 shows an RBS plot of film No. 20. The plot is the number of counts versus energy of the back scattered α -particles. Since Ge has higher mass than Si, particles backscattered from Ge atoms will have a higher energy than those scattered from Si atoms. Thus, the Ge content profile appears first at the right of the chart. Starting at about the fourteenth layer (seven Si and seven SiGe layers), the sum of the Ge and Si signals causes a sharp rise of the count level. The periodicity of the Ge signal is very clear up to at least 28 layers. Since the data are collected in parallel, the measurement should not be affected by drift in the beam current. The fluctuation seen in the signal is thus most probably real and may be due to fluctuation in the RF power during growth which has been noticed. The Ge content measured by RBS is ~ 10 percent.

The Auger depth profile is made by periodic measurement as the sample is being sputtered by argon ion bombardment. The nominal sputtering rate is about $1000\text{\AA}/\text{min}$. The silicon signal rather than the germanium peak was used. Although measuring the fluctuation of the principal constituent is subject to magnification of errors, it was determined that this method would yield better results by obtaining better signal-to-the-noise ratio since Ge has a very low Auger sensitivity. Figure 8 shows the relative magnitudes of the Si and Ge signals of sample No. 20. The Ge content of the alloy layers was determined to be 14.6 percent, which corresponds fairly well to the 6.5 percent average Ge content of the multilayer structure determined by EDXS (the ratio should be 2:1 if the multilayer film thicknesses are identical). Figure 9 is a plot of sputtering time vs Si Auger signal level and shows the fluctuation of the percent Si content of the first 14 layers of Sample No. 20 showing a slight reduction in signal level for the deeper layers, most likely due to drift in the electron beam current.

It appears from the AES data that there is a transition region at the layer interfaces where the Si content (hence also Ge content) changes gradually. The width of this transition region is about 100\AA near the surface and increases to almost half the layer thickness at greater depth (see Figure 9). The finite width of the transition region can be attributed to several factors: insufficient purging of the reactant gases between the growth of each layer, insufficient reactant gas mixing when their flow is turned on after each purge period, or it may be an artifact of the profiling technique as a result of mixing by recoil of target atoms (Si or Ge) during sputter etching. We tend to

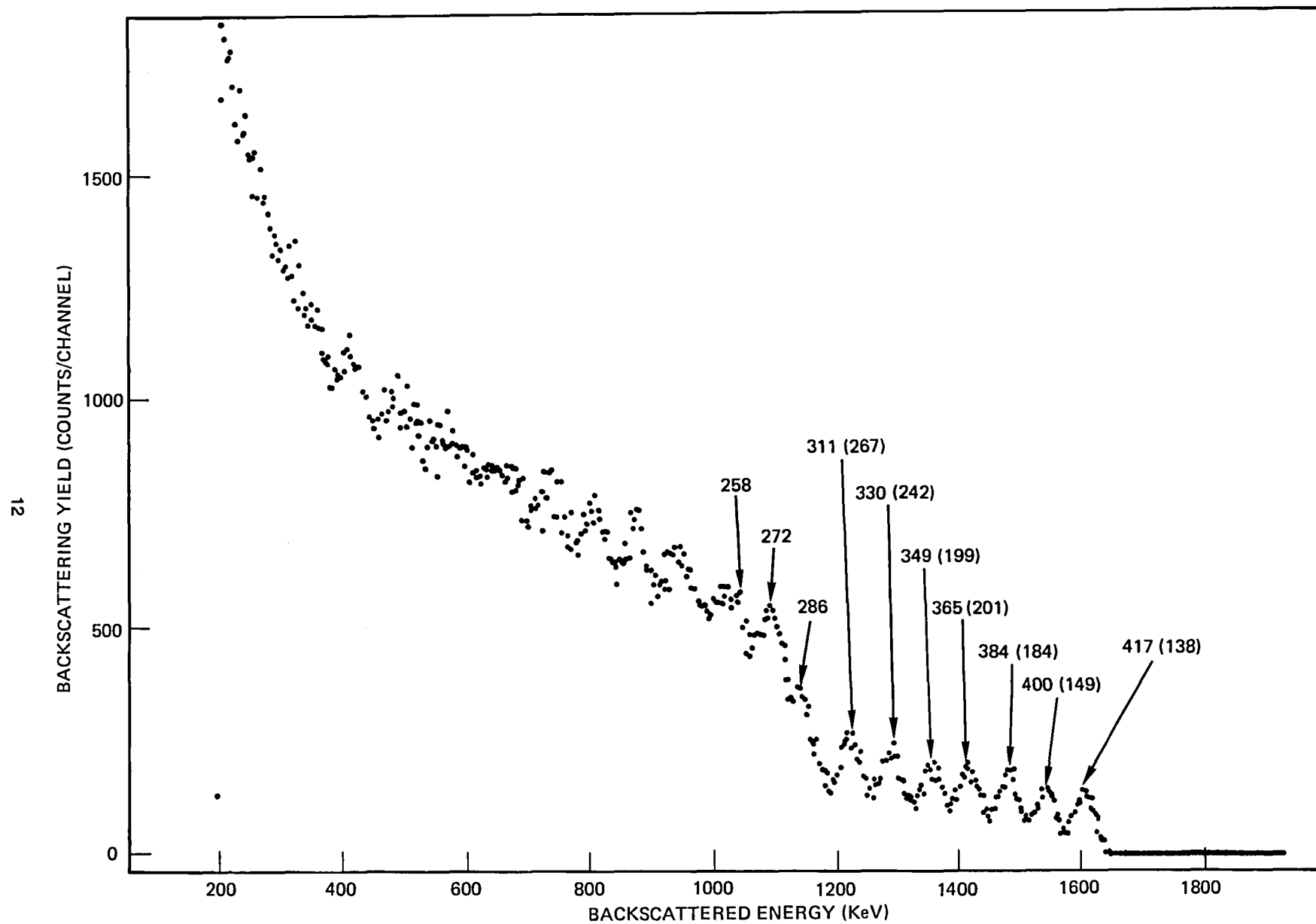


Figure 7. Rutherford Back Scattering Profile of Film No. 20. The Ge Signal of the First 14 Layers (Si and SiGe) is Seen at the Right; the Si Signal is added to the Ge Signal at the Left.

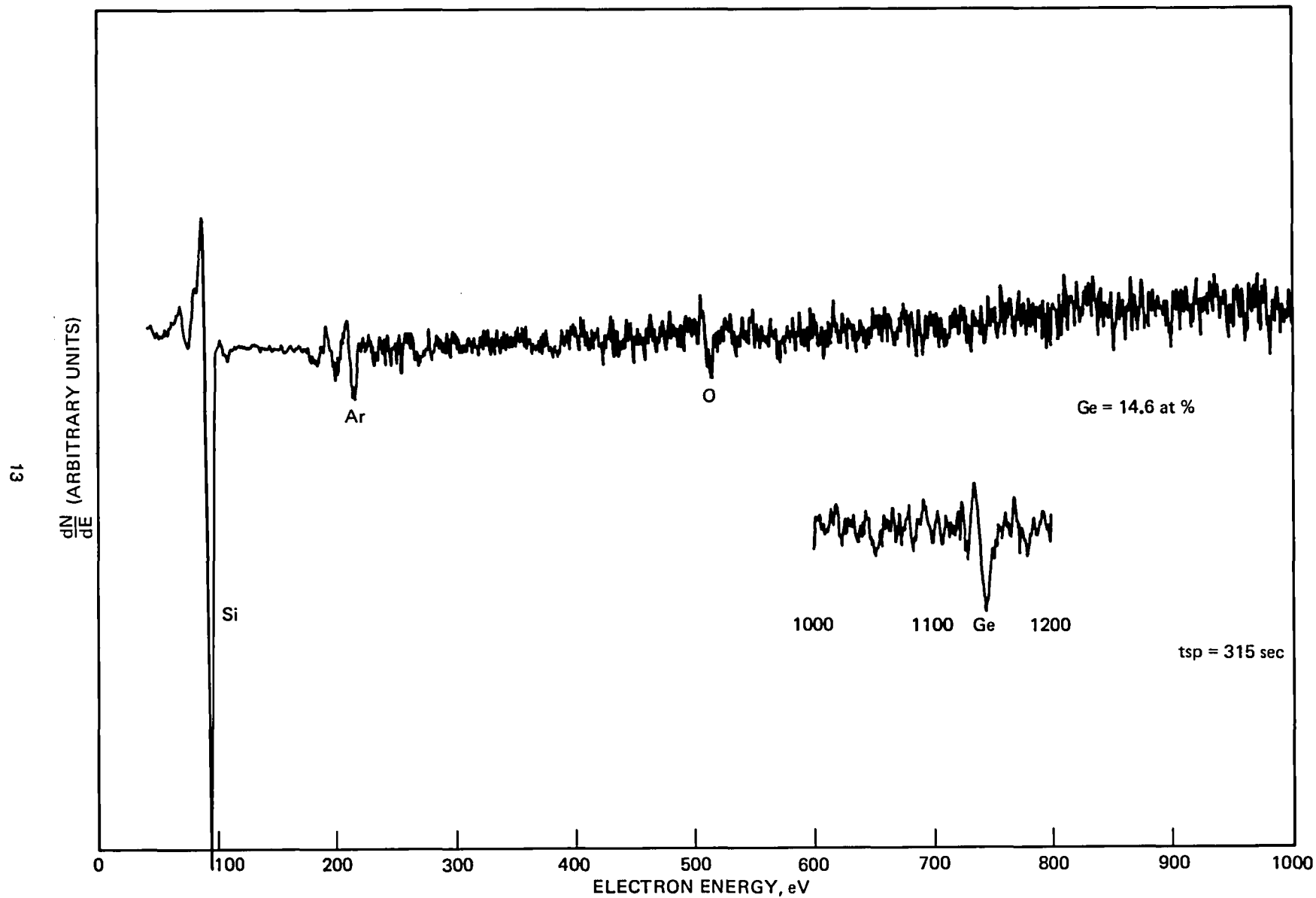


Figure 8. Auger Signal of Si and Ge in Film No. 20

#20 (RUN 2)

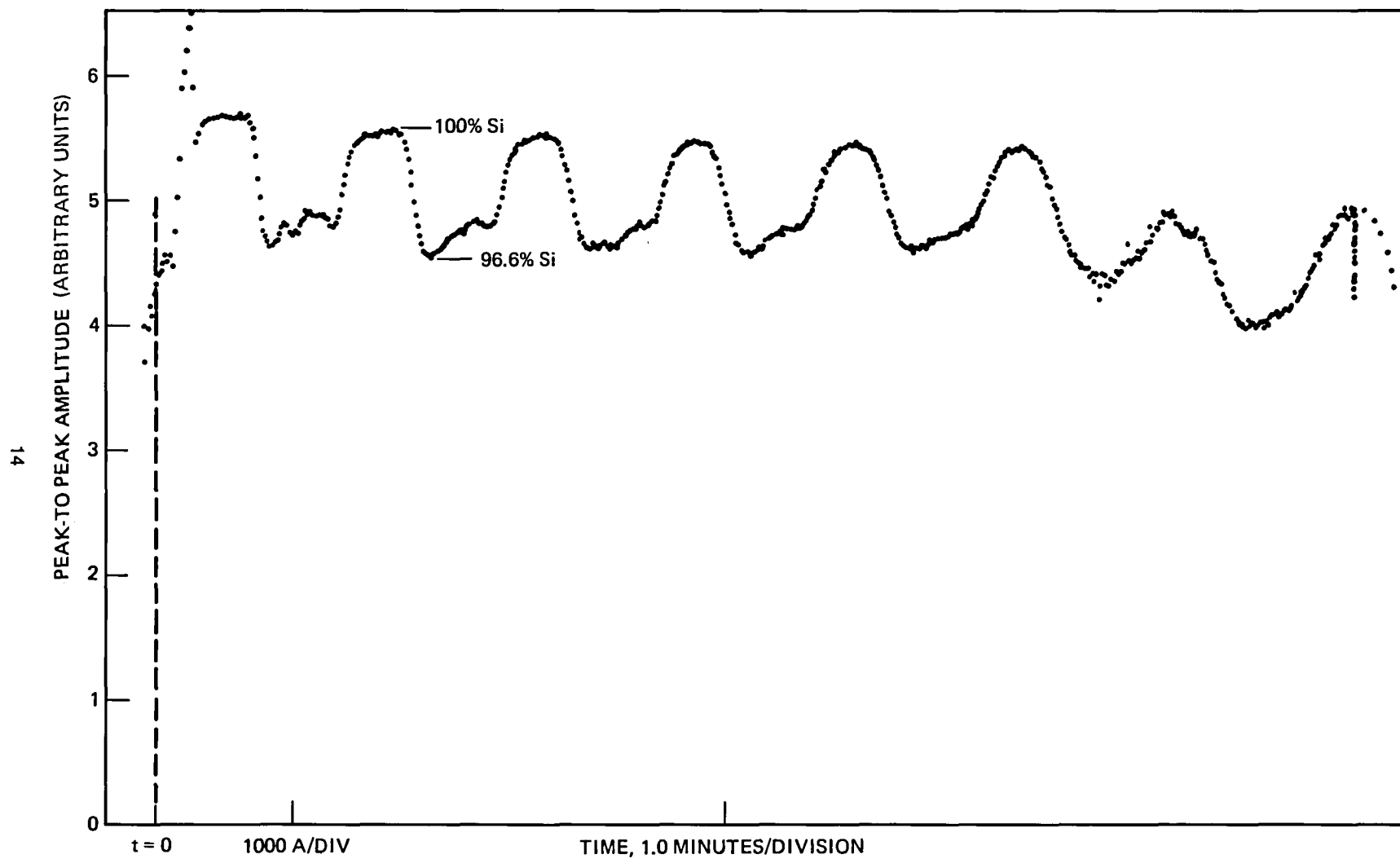


Figure 9. Auger Signal of Si Versus Sputtering Time For Multilayer Sample No. 20. Sputtering Rate is About 100 Å/Min.

consider the later factor to be the dominant one in light of the broadening of the apparent transition layer width with depth, since mixing caused by sputter etching increases with etch time. Furthermore, the data obtained from the carrier concentration profile experiment, to be discussed in the next chapter, favors the picture of well defined interfaces between layers, at least for the SiGe:Si interfaces (SiGe on top of Si). Another factor that was ruled out concerning the broadening of the transition region is elemental Si and Ge interdiffusion between layers. Calculations based on Ge diffusion in Si indicate the transition layer width should be less than 30Å for the growth condition of the films.

SIMS analysis was made to examine the possibility of dopant (phosphorus) pile up at the interfaces. This possibility was raised in conjunction with the results obtained from the carrier concentration profile experiment. SIMS analysis showed no pile up of phosphorus or any other dopant at the interfaces. The analysis, however, indicated that the phosphorus concentration in the alloy layer is about 1/2 to 1/3 that in the Si layer in spite of the fact that the flow rate of phosphorus was kept constant during the growth of both layers. This result might indicate lower incorporation rate of the phosphorus atoms in the alloy layer due to the fact that the size of phosphorus atom is much closer to Si than Ge. Phosphorus atoms should thus fit more readily into the Si lattice than into the lattice of the SiGe alloy. Due to the relatively low concentration of dopants in the films ($\sim 10^{16}\text{cm}^{-3}$), each data point required considerable sputter time resulting in lower depth resolution. Dopant measurements were made at only a few points during the film analysis. The Si and Ge content were very well resolved. The data for Film No. 27 is shown in Figure 10. Again, the argument for the transition region between layers in AES also applies to SIMS.

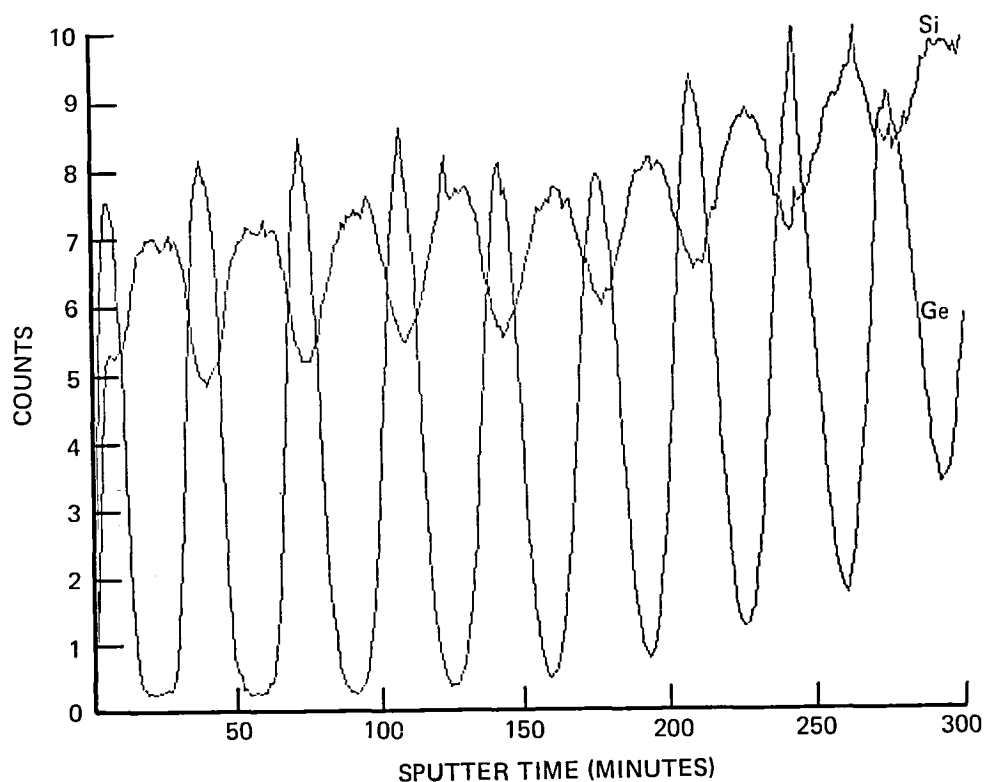


Figure 10. SIMS Profile of Sample No. 27

Double Crystal X-Ray Diffraction Rocking Technique

The double crystal x-ray rocking technique is an accurate method of measuring the lattice constants of crystals and in particular, for measuring small differences of lattice constants that exist between an epitaxial film and the substrate.

The measurements were made under three sets of conditions. First, using FeK α x-rays and a Si (400) first crystal, the rocking curves of the symmetric (400) reflection from the samples were recorded. CuK α x-rays and a Ge (333) first crystal were used to obtain the rocking curve for the (422) reflection from the samples. These reflections are asymmetric and the rocking curves were recorded for both senses of asymmetry. The strong diffraction peak from the Si substrate was used as an interval standard based on a lattice parameter for Si of 5.4301Å. The locations of the centers of the other diffraction peaks were measured relative to the Si peak. In this way the lattice parameter normal to the plane of the film is easily calculated from the Bragg equation for (400) diffraction. The lattice parameter in the direction normal to the (422) planes, which is 35 degrees from the normal, can be calculated from the peak positions in the two different (422) rocking curves. Then using the isotropic elasticity equations, the free lattice parameters of the film (that is the lattice parameters which it would exhibit if it were not strained) can be calculated. After this, the residual strain in the film is determined, and assuming a linear variation of the lattice parameter with Ge content the alloy composition can be determined. A set of three samples were first measured. The film parameters are listed in Table 3.

Qualitatively, all rocking curves contained a strong, relatively sharp peak which is assumed to be the diffraction peak from the Si substrate. (A sample rocking curve is shown in Figure 11) Also, all rocking curves contained a weaker, broader peak at a lower value of glancing incident angle than the substrate peak. It is assumed that this weaker, broader peak is due to diffraction from the alloy film. For the two multilayer samples, some rocking curves also contained a weak, broad peak at a higher value of glancing incident angle than the substrate peak. It is assumed that these extra peaks are produced by diffraction from the intervening Si films.

Quantitative results are summarized in Table 3. The x-ray analysis gives the unstrained lattice parameter and the strain in the film. The unstrained lattice parameter is characteristic of the composition of the film and is used to derive the Ge content. The strain is expressed in terms of its in-plane component. This strain is compressive and, therefore, negative. The strain relief is calculated by comparing the measured in-plane strain with the strain expected if a film having the unstrained lattice parameter were elastically deformed to match the Si substrate. This definition is

Table 3. Si-Ge Alloy — X-Ray Strain Results

SAMPLE		UNSTRAINED LATTICE PARAM (Å)	Ge CONTENT (ATOMIC %)	IN-PLANE STRAIN (X10 ⁻⁴)	STRAIN RELIEF (%)
152	5 LAYERS	5.4673	16.3	- 6.3	91
229	1 LAYER	5.4652	15.4	- 7.4	88
234	63 LAYERS	5.4600	13.1	-30.5	44

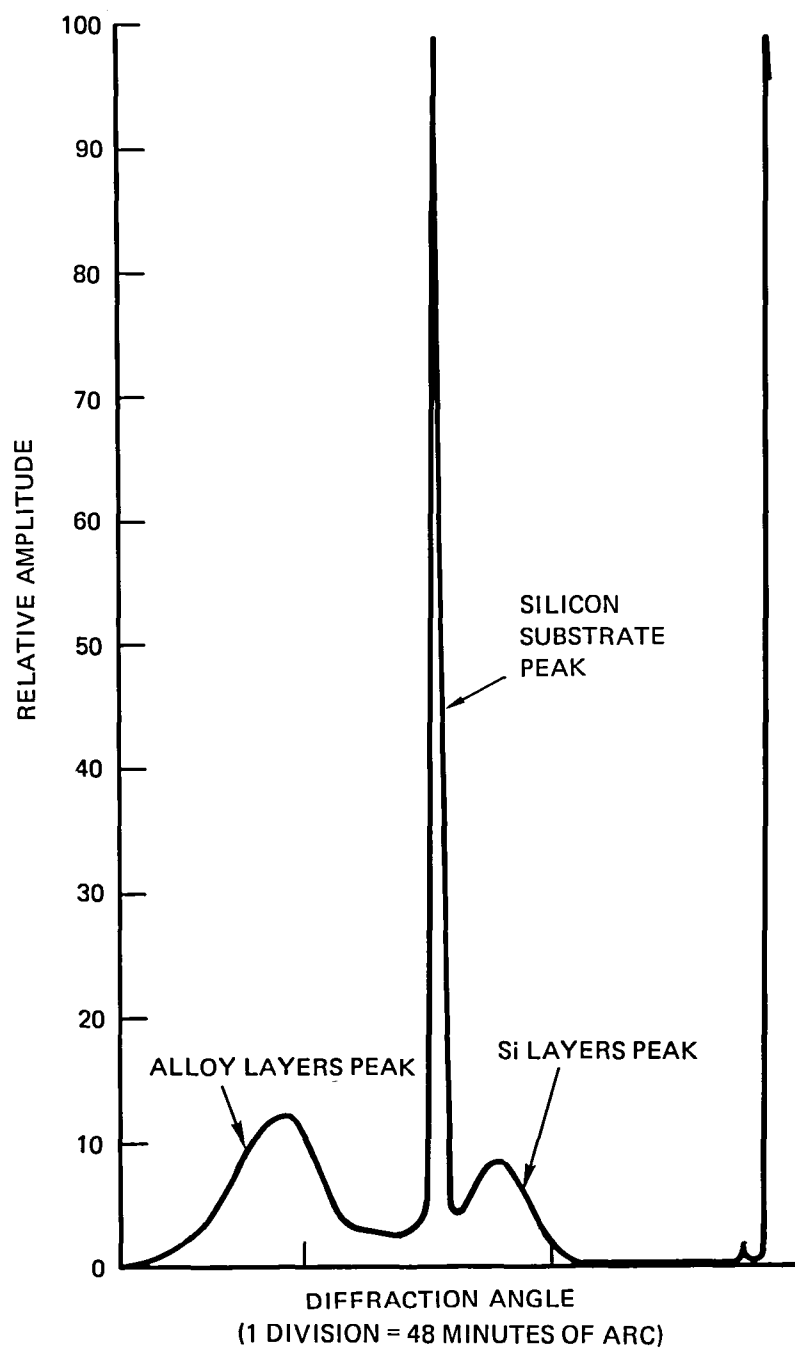


Figure 11. Rocking Curve of Sample 234 for Reflection Off the (422) Planes

not very accurate since the alloy layers are grown in Si layers that might be themselves elastically strained. Sample 234 was the only one to have very distinct extra peaks. These were observed in the symmetric and in one of the asymmetric rocking curves. If we assume that in the other asymmetric rocking curve the extra peak was hidden within the other peaks, then the extra peak can be ascribed to the intervening layers of Si with a small amount (<3 percent) of Ge exhibiting in-plane tensile strain of about 0.2 percent.

The quantities in the table are averages in the sense that the diffraction peak position is an average of the diffraction parameter of the film. To this extent, the uncertainty in each quantity is in the last significant figure shown. However, the diffraction peaks are fairly broad. The widths of these peaks could be due to a Ge content which varies from 13 to 18 percent and a strain which varies from -11×10^{-4} to about zero.

This brings us back to the question of strain relief in the alloy layers which was calculated by subtracting the measured in-plane lattice constant from that of the Si substrate. The actual strain relief in a multilayer film, however, should be equal to the difference between the in-plane lattice constants of the SiGe and the Si layers. In film No. 234 the average in-plane lattice constant is $\sim 5.4436\text{\AA}$. This gives strain relief of only 16 percent rather than 44 percent as calculated previously. It should again be pointed out that the strain distribution is quite large as seen in the width of the diffraction peak and thus the above argument should be considered in light of this fact.

The data also indicate that the strain relief in a single alloy layer (film No. 229) and multilayer film with relatively thick alloy layers (No. 152) is considerably larger than that in the multilayer film with thinner alloy layers (No. 234). This agrees well with published theoretical (Ref 13) and experimental (Ref 14) work indicating that thin epitaxial layers with small lattice mismatch to the substrate can be grown with few interface dislocation provided that they are thin enough. Intervening layers of the same lattice constant as the substrate can lead to similar results as seen in the present case.

We thought of examining that question further by measuring the strain in the single layer films. Two samples with 500\AA alloy films were prepared. One film was grown on bare Si (No. 275) and the other (No. 277) on an epitaxial Si buffer layer grown immediately before it. The results shown in Table 4 confirm the conjecture that the strain relief is primarily affected by the layer thickness. Here the strain relief was even smaller than that of film No. 234. It should be pointed out that the uncertainty in the strain measurements is quite large ($\sim \pm 20$ percent) due to the broadness of the diffraction as illustrated in the rocking curve shown in Figure 11.

Table 4. X-Ray Strain Results of Thin Single Layer SiGe Alloy Films

<u>SAMPLE</u>	<u>UNSTRAINED LATTICE PARAM (\AA)</u>	<u>Ge CONTENT (ATOMIC %)</u>	<u>IN-PLANE STRAIN ($\times 10^4$)</u>	<u>STRAIN RELIEF (%)</u>
275	5.4579A	0.122	-0.0041	+20%
277	5.4588A	0.126	-0.0068	-29%

TEM and SEM Examination

Several films were examined by transmission electron microscopy by Dr. D.K. Sadana of the Lawrence Berkeley Laboratory. The films examined are listed in Table 5. A cross section image of the multilayer film No. 234 is shown in Figure 12. The first five to seven layers closest to the substrate are very uneven and might be discontinuous. The layer structure becomes more even away from the substrate, eventually becoming regular and fairly planar. The unevenness close to the substrate interface is consistent with the observation during film growth that the film starts with a grayish look and gradually becomes more reflective as the growth proceeds. This growth pattern is characteristic of initial growth nucleation in isolated islands that grow and coalesce until the growth covers the whole surface. The uneven part of the film seen here is about seven layers (Si + SiGe) or about 5000Å. The observation that the mobility seen in thin films ($<1.0\mu\text{m}$) is considerably lower than that in thicker films might be due to the unevenness of a substantial part of the film in the thinner films.

Table 5. Summary of Parameters of Films Examined by TEM

FILM NO.	GROWTH TEMP °C	TOTAL THICKNESS MICRONS	NO. OF LAYERS	μ CM ² /VOLT SEC	ρ OHM CM	N CM ⁻³
234	1002	4.5	63	1440	0.19	2.3×10^{16}
250	1006	3.2	1	430	0.21	7.0×10^{16}

The crystalline quality of the film seems to be fairly good with a moderate number of dislocations (marked by dotted lines in the picture). Figure 13 shows a TEM picture normal to the plane of a single layer film for a region close to the thinned out crater in film No. 250. Misfit dislocations are evident (straight crossed lines) along the [100] and [010] directions.

Typical surface morphology of the multilayer films is seen in Figure 14. Cross hatched slip lines are seen in all our samples and are thought to be generated during the cooling period of the film after growth due to the difference between the thermal expansion coefficient of the alloy layer and that of the Si substrate.

Summary

1. The multilayer film structure is seen to have fairly abrupt layer interfaces ($<100\text{\AA}$).
2. The dopant density (phosphorus) in the alloy layer is about 1/3 to 1/2 that in the Si layers indicating lower incorporation rate of phosphorus into the alloy layer than the Si layer during film growth. Within the experimental uncertainty of the SIMS technique, no dopant pile-up is observed at the layer interfaces.
3. The mismatch between the lattice constants of the alloy layer and Si is accommodated through both elastic strain and strain relief defects (e.g., dislocations). The elastic strain, however, in multilayer or thin single layer alloy films is considerably larger than in thick alloy layers and consequently thin layered films are expected to have fewer dislocations.
4. The growth of the first layers of multilayer films appears to be uneven. This observation explains the lower mobilities seen in thin multilayer films ($<1.0\mu\text{m}$).

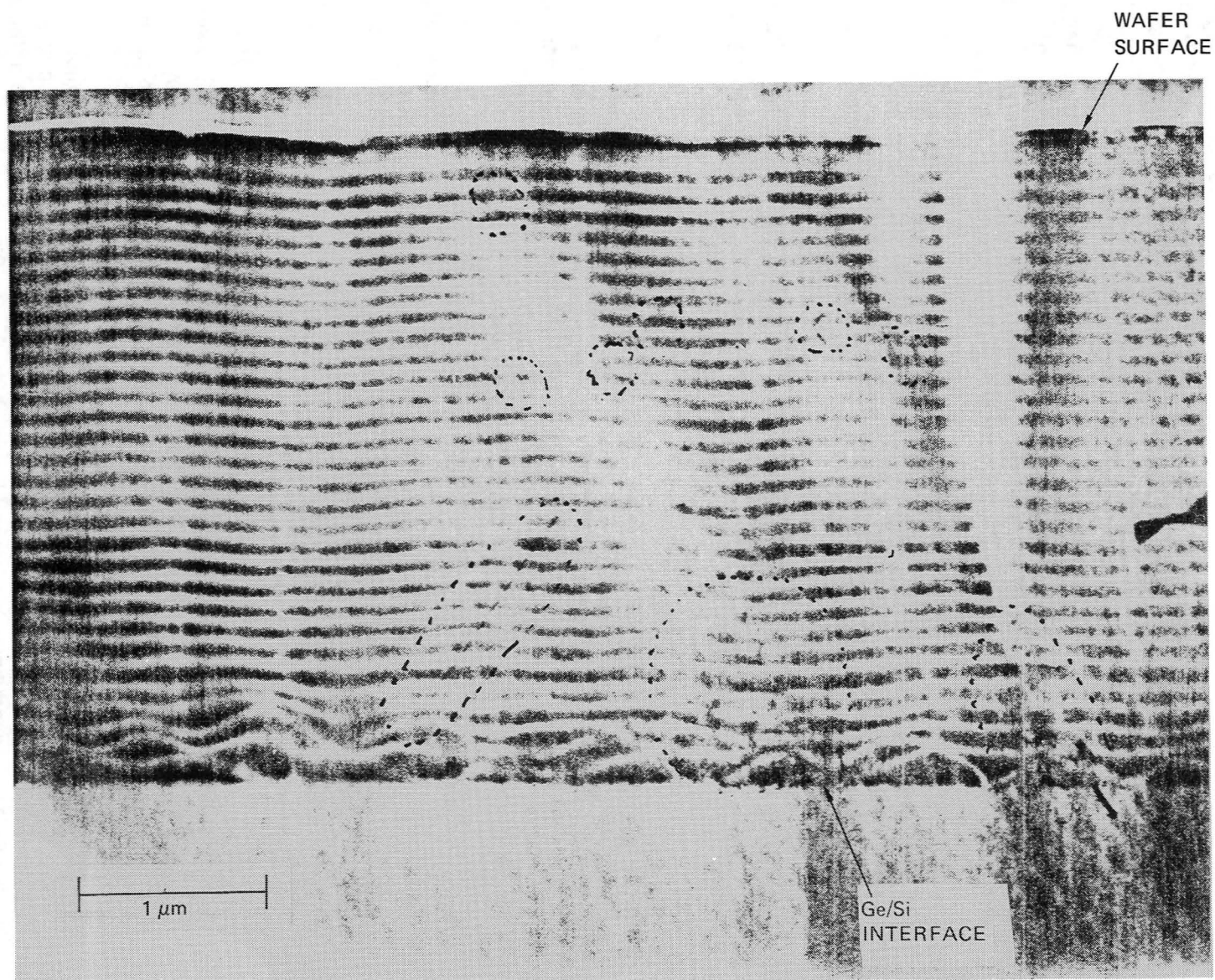


Figure 12. TEM Micrograph of the Cross Section of Film No. 234

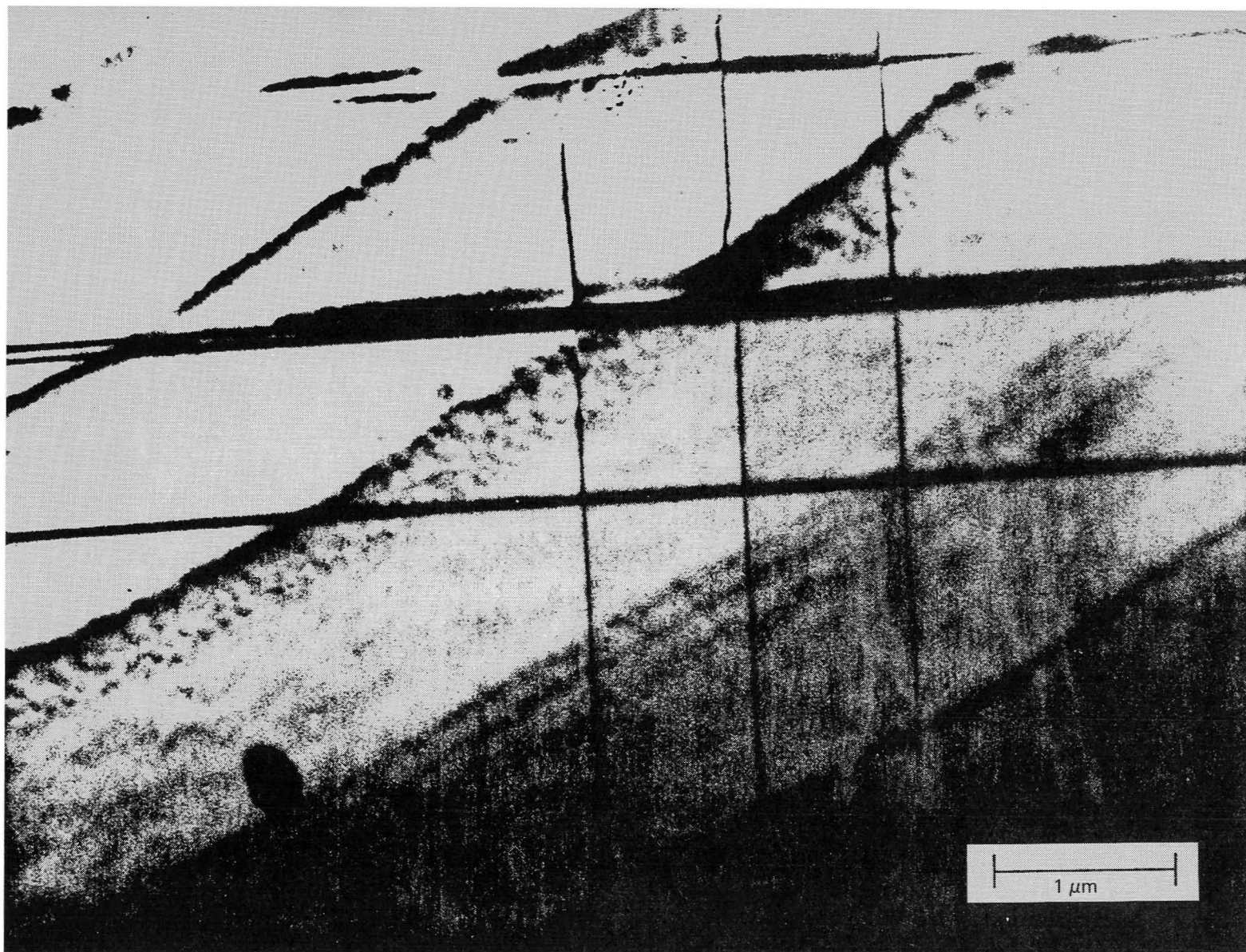


Figure 13. TEM Micrograph Through a Thinned Section of Film No. 250. The Vertical and Horizontal Lines are Dislocations.

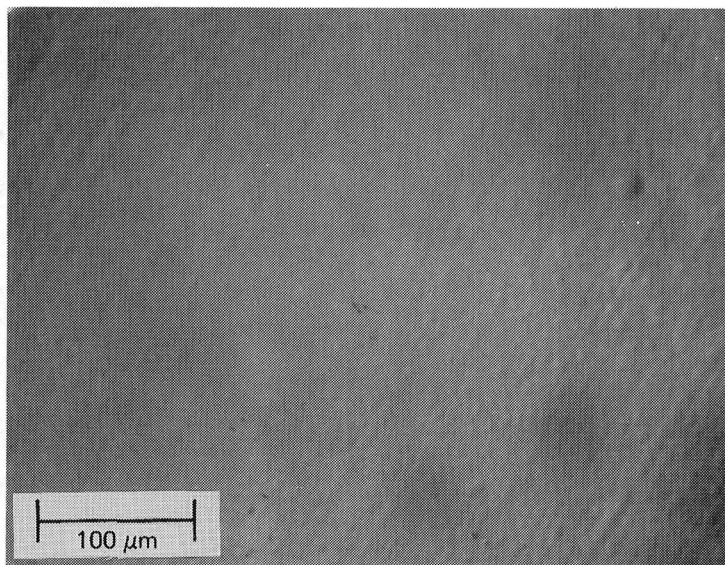


Figure 14. Microphotograph of the Surface of Film No. 172 Showing the Surface Morphology
Notice the Cross Hatch Pattern Along the (100) and (010) Directions

SECTION IV

ELECTRICAL CHARACTERIZATION OF THE FILMS

The organization of the material in this section follows the chronological order of the experiments performed. The investigation of the electrical properties started with Hall and conductivity measurements in the temperature range of 77°K to 400°K. These measurements gave an average of the mobility and carrier concentration in the films. The results showed significant and unusual differences between the carrier concentration temperature dependence in the multilayer sample compared to that in single layer Si or SiGe films. The measurements were extended to lower temperature (20°K) which revealed non-freezout of carriers. Experiments were then made to determine the carrier concentration profile in the film using C-V measurement of Schottky diodes fabricated on the films. This in turn showed very interesting features in that the carrier concentration (n) was strongly modulated with depth and that its peaks increased sharply at low temperatures. It also confirmed the carrier non-freezout which occurs at these peaks.

The above results prompted the design of an experiment to measure drift and Hall mobilities and the carrier concentration profiles in the film using what is known as a gated Hall device (GHD). This is simply a field effect transistor with tabs along the channel for measuring the potential drop along the direction of the current flow, and normal to the current flow (Hall voltage). The measurements showed that the drift mobility is also modulated with depth and that the peaks are very close to the peaks in the carrier concentration profile. The Hall mobility showed a similar trend, but with large data scatter. In all, the data gathered so far point to electron confinement at the alternate layer interfaces and the possibility of mobility enhancement as a result of this confinement as will be discussed in more detail later in this report.

Hall Mobility and Carrier Concentration Temperature Dependence

Hall measurements were made using the Van der Pauw technique. The samples were rectangular in shape and about 5 to 10 mm on the sides. The contacts were made with indium dots in about the middle of each edge. The indium contacts were alloyed for a few minutes at 400°C in N_2 . The measurements were made first between 77°K and 400°K in a set-up equipped with a liquid nitrogen dewar and with a resistance heater that surrounds the sample holder to control the temperature. The results obtained for multilayer film No. 39, a single layer SiGe film No. 75, and a single layer Si film No. 77, are shown in Figures 15, 16 and 17 respectively.

The Si and SiGe single layer films showed 'normal' behavior; i.e., the carrier concentration remains constant over a range of temperatures where the donors are fully ionized, then it starts to decrease as $\exp - \frac{\Delta E}{2kT}$ with $\Delta E = 43$ meV. Here we assumed that the semiconductor is not heavily compensated. i.e.,

$$N_D > n \gg N_A .$$

The activation energy of the donors (ΔE) is much closer to that of phosphorus (P) in Si than the activation energy of P in Ge which is about 12 meV. This might lead to the conclusion that the donor ionization energy is dependent only on the average alloy composition rather than the nature of the neighbors to the P atom.

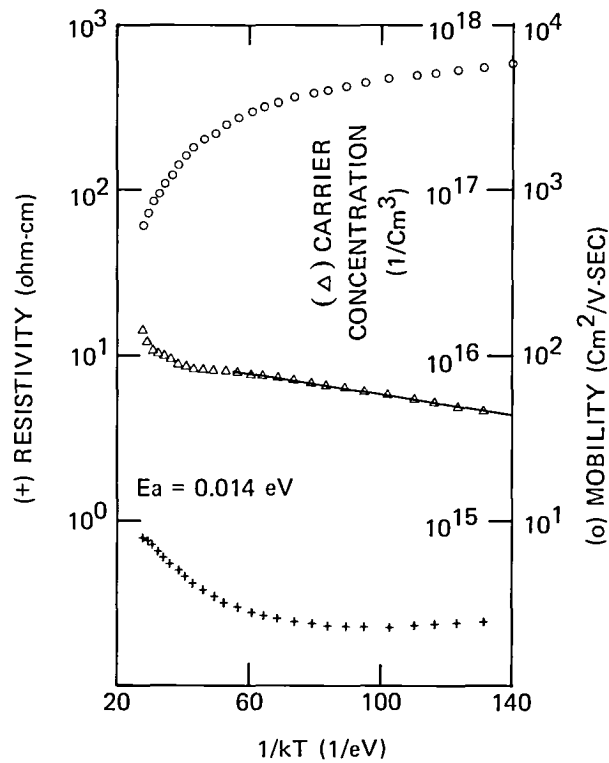


Figure 15. Resistivity (+), Carrier Concentration (Δ) and Carrier Mobility (o) in Multilayer Si/SiGe Film No. 39 (n-Si/SiGe on p-Si)

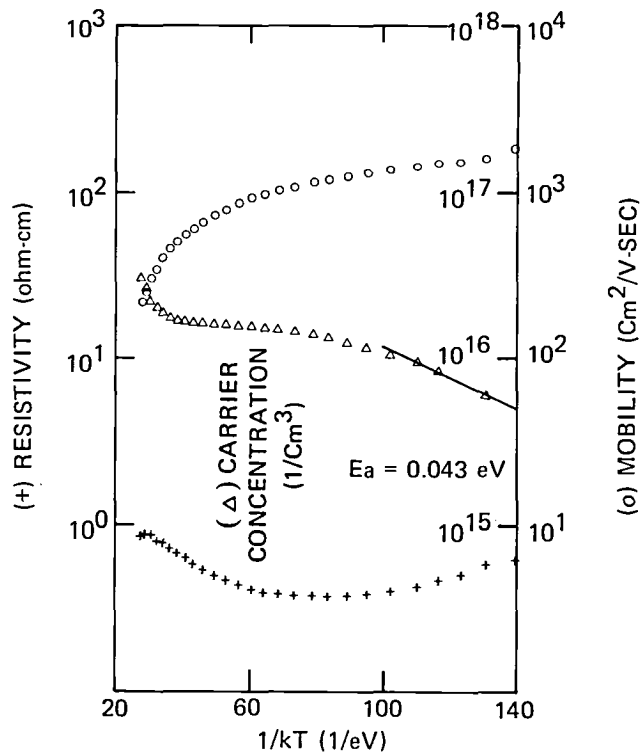


Figure 16. Resistivity (+), Carrier Concentration (Δ) and Carrier Mobility (o) of Single Layer SiGe Film No. 75 (n-Si_{0.85}Ge_{0.15} on p-Si)

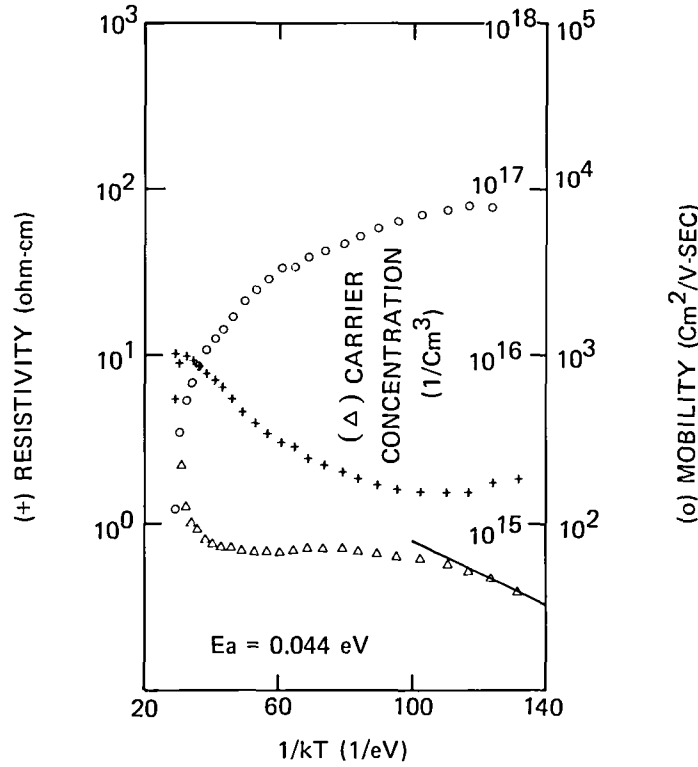


Figure 17. Resistivity (+), Carrier Concentration (Δ) and Carrier Mobility (o) of Single Layer Silicon Film No. 77 (n-Si Epi on p-Si Substrate)

Now looking at the multilayer films, we found that n varies much slower at low temperature than in single layer films. In fact, the slope of $\log n$ vs. $\frac{1}{kT}$ corresponds to an “activation energy” of about 14 meV.

The measurements were extended to much lower temperatures in a set up equipped with a helium refrigeration unit capable of reaching 10°K at the sample holder. The results are summarized below:

The measurements were made on five multilayer samples whose physical properties, growth conditions and electrical properties at room temperature are summarized in Table 6. All five samples were grown at temperatures close to 1000°C but with different total film thickness and with different total number of layers. Sample No. 194 contains a 2.5 μ m p-type buffer layer between the substrate and the Si/SiGe multilayer. The other four samples were grown directly on the p-type (100) Si substrate. The electrical properties have been measured at room temperature using both the standard Hall measurement and Van der Pauw techniques. There is a small difference in the results of these two techniques as shown in Table 6. Such a small difference may come from the inhomogeneity of the sample.

Temperature dependence of the resistivity measured between room temperature and 19.7°K for three multilayer Si/SiGe samples (No. 219Ge, No. 218Ge and No. 219Ge) is shown in Figure 18. These samples were grown at $1002 \pm ^\circ C$ with approximately constant thickness per layer ($\sim 1000\text{\AA}/\text{layer}$). The total number of layers are 45, 29 and 13 for No. 213Ge, No. 218Ge and No. 219Ge, respectively. The most important result obtained in this investigation is that resistivity

Table 6. Summary of Properties of Multilayer Si/SiGe Films Measured Below 20° and 400°K

SAMPLE NUMBER	TOTAL THICKNESS (μM)	NUMBER LAYERS	LAYER THICKNESS (\AA)	GROWTH		HALL EFFECT			VAN DER PAUW		
				TEMP ($^{\circ}\text{C}$)	TIME (MIN)	N 10^{16} CM^{-3}	$\mu \text{ CM}^2/\text{V-SEC}$	$\rho \text{ OHM-CM}$	N 10^{16} CM^{-3}	$\mu \text{ CM}^2/\text{V-SEC}$	$\rho \text{ OHM-CM}$
194	1.1	21	523.8	1002	0.6	0.93	1453	0.4625			
210	4.4	91	483.5	1004	0.4	1.093	1157	0.4942	0.865	1437	0.503
213	4.3	45	955.6	1004	0.8	1.02	1463	0.419	1.066	1382	0.424
218	2.8	29	965.5	1000	0.8	0.911	1212	0.566	1.102	1299	0.4362
219	1.4	13	1077	1002	0.8	1.24	1179	0.4274	1.10	1307	0.4344

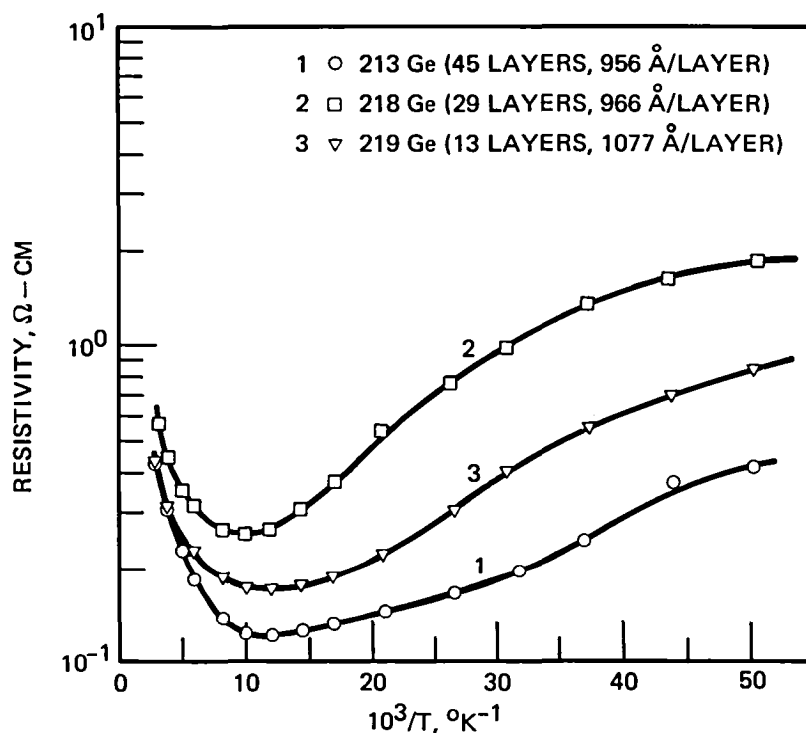


Figure 18. Resistivity Versus $1/T$ for Three Multilayer Si/SiGe Samples all Grown at $1002 \pm 2^{\circ}\text{C}$ with Approximately Constant Thickness Per Layer ($\sim 1000\text{\AA}$) but Different Total Number of Layers

changes very little between 300°K and 19.7°K for all five samples measured. This slow change in resistivity with temperature was found to be a result of non-freezout of free carriers at low temperatures as seen in Figure 19. This result is drastically different from a typical uniformly doped n-type Si semiconductor material. In general, an n-type uniformly doped bulk Si sample with resistivity at room temperature comparable to the three samples above will have almost seven orders of magnitude change in resistivity in the same temperature range.

The corresponding temperature dependence of the Hall mobility measured for the same three samples is shown in Figure 20. For the sake of comparison only, the Hall scattering factor was taken to be unity.

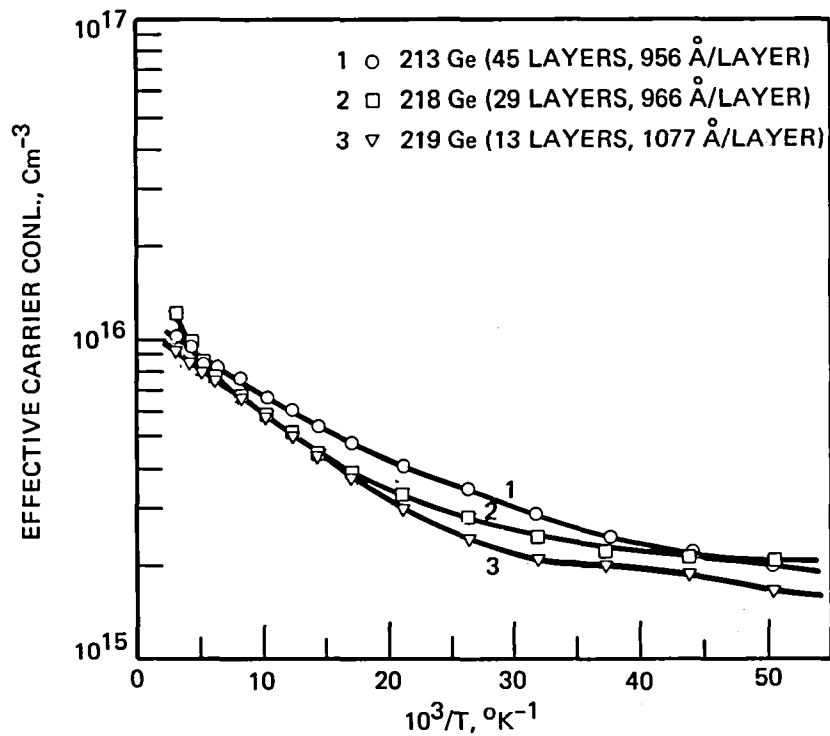


Figure 19. Effective Carrier Concentration Versus 1/T for the Three Multilayer Si/SiGe Samples of Figure 17.

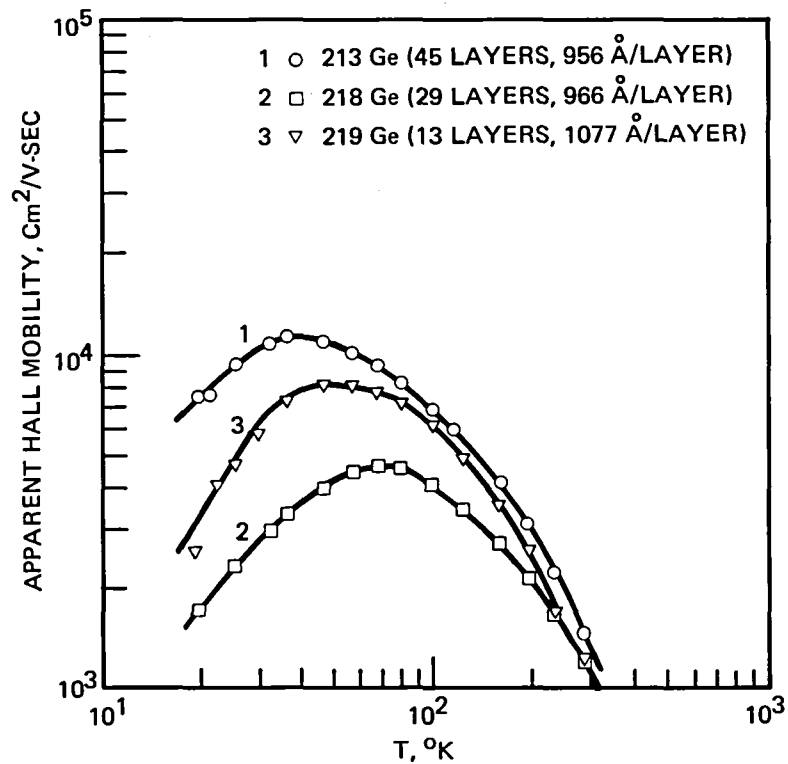


Figure 20. Temperature Dependence of Mobility for the Three Multilayer Si/SiGe Samples of Figure 17.

Figure 19 shows that the effective carrier concentrations in all three samples measured are almost equal over the entire temperature range. The difference in resistivity (see Figure 18) comes mainly from the mobility variation among these three samples as indicated in Figure 20. It was also found that the small mobility difference at room temperature was enlarged at low temperature. However, no apparent trend was observed as the total number of layers reduced from 45 layers (No. 213Ge) to 29 layers (No. 218Ge) to 13 layers (No. 219Ge). Mobility of the 45 layer sample is higher than either the 29 or 13 layer sample, but the mobility of the 29 layer sample is lower than that of the 13 layer sample. The large change in mobility was apparently not due to concentration variation of the major n-type dopant since all three samples have about the same free carrier concentration (Figure 19), but is very likely caused by some unknown acceptors which would strongly affect the mobility, especially at low temperature.

Figure 21 compares the resistivity vs $1/T$ curves for two multilayer Si/SiGe samples. Both were grown at the same temperature (1004°C) and with about the same total thickness ($\sim 4.4\mu\text{m}$), but with different thickness per layer. Sample No. 213Ge has about twice the thickness per layer as sample No. 210Ge. Again, it is found that resistivity at 20°K is about the same as that at room temperature for the multilayer Si/SiGe samples. The temperature dependence of Hall mobility for the same two samples is shown in Figure 22. It indicates that mobility is higher for the sample with thicker layers (No. 213Ge).

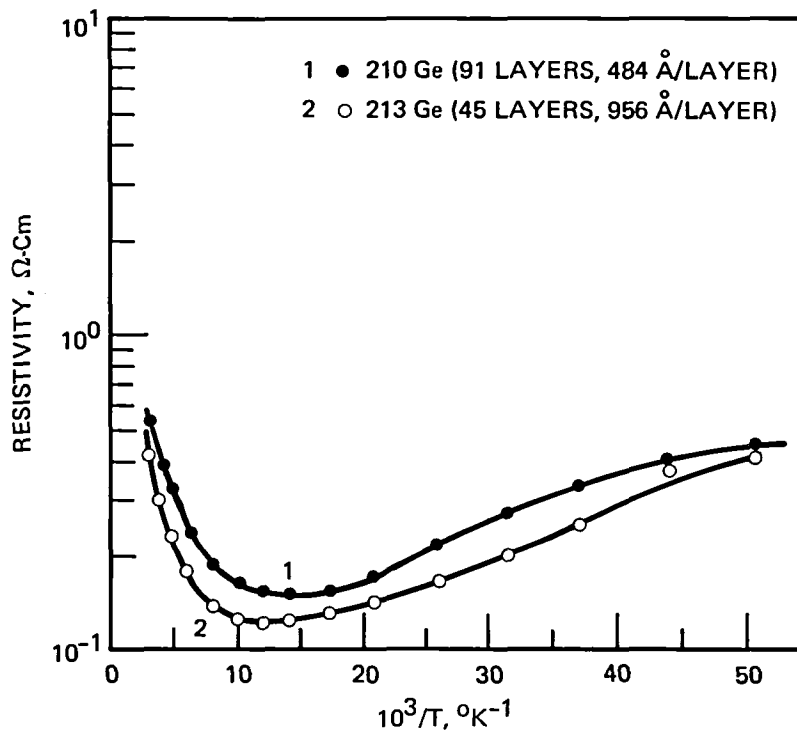


Figure 21. Resistivity Versus $1/T$ for Two Multilayer Si/SiGe Samples Both Grown at 1004°C and with About the Same Total Thickness ($\sim 4.4\mu\text{m}$) but Different Number of Layers.

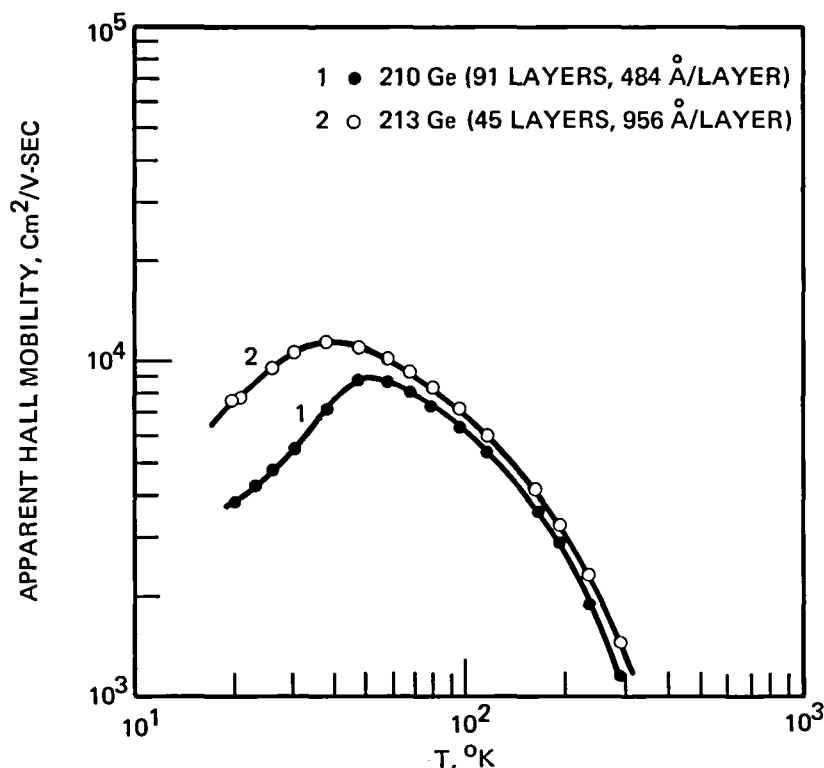


Figure 22. Temperature Dependence of Hall Mobility for the Two Multilayer Si/SiGe Samples of Figure 20.

Figure 23 shows the resistivity vs $1/T$ curve for multilayer Si/SiGe samples containing a $2.5\mu\text{m}$ p-type buffer layer between the substrate and the multilayers. The temperature insensitive resistivity measured between 298°K and 19.7°K again was found to be coming from a non-freezout of free carriers at low temperature. Mobility of this sample is compared in Figure 24 with a sample without buffer layers and with a film thickness per layer twice as high. Higher mobility is found at low temperature for the sample with the buffer layer.

In summary, the most significant result obtained in the measurements is that non-freezout of free carriers is observed for all five multilayer Si/SiGe samples being measured. The following tentative conclusions are also obtained from the limited samples being studied:

1. For samples with constant thickness per layer, increasing layer number may improve film quality.
2. For samples with constant total thickness decreasing layer number may improve film quality.
3. Samples with buffer layers may have better film quality.

Carrier Concentration and Mobility Profiles

The non-freezeout of carriers at low temperature seen in multilayer films brings to mind the phenomena of carrier transfer across the heterojunction from the higher conduction band side to the lower conduction band side. This phenomenon occurs in the GaAs-GaAlAs heterojunction and is responsible for the observed enhanced mobility in the modulation doped heterostructure (Ref 1).

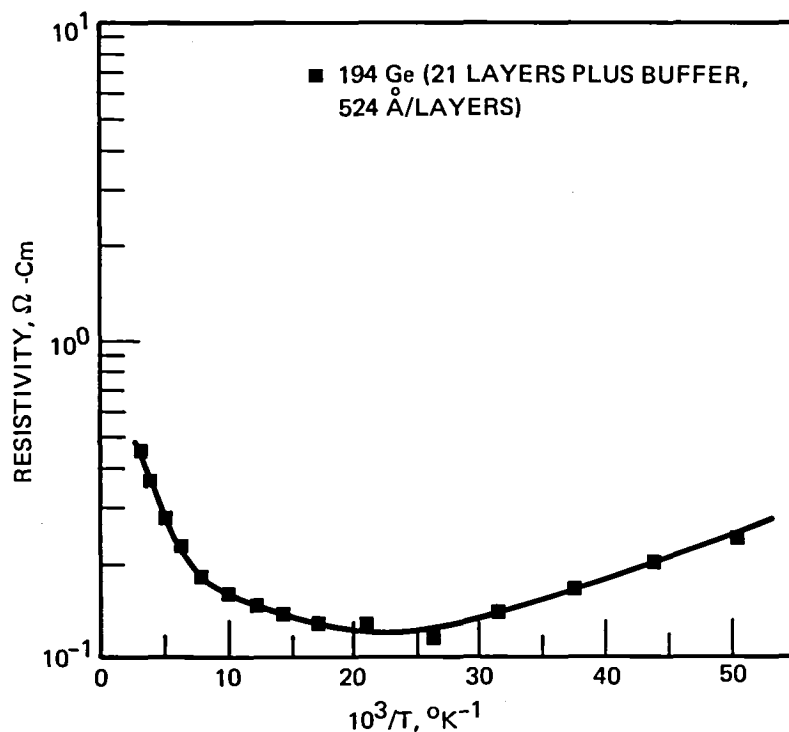


Figure 23. Resistivity Versus $1/T$ for Multilayer Si/SiGe Sample Containing a $2.5\mu\text{m}$ P-Type Buffer Layer Between the Substrate and the Multilayer.

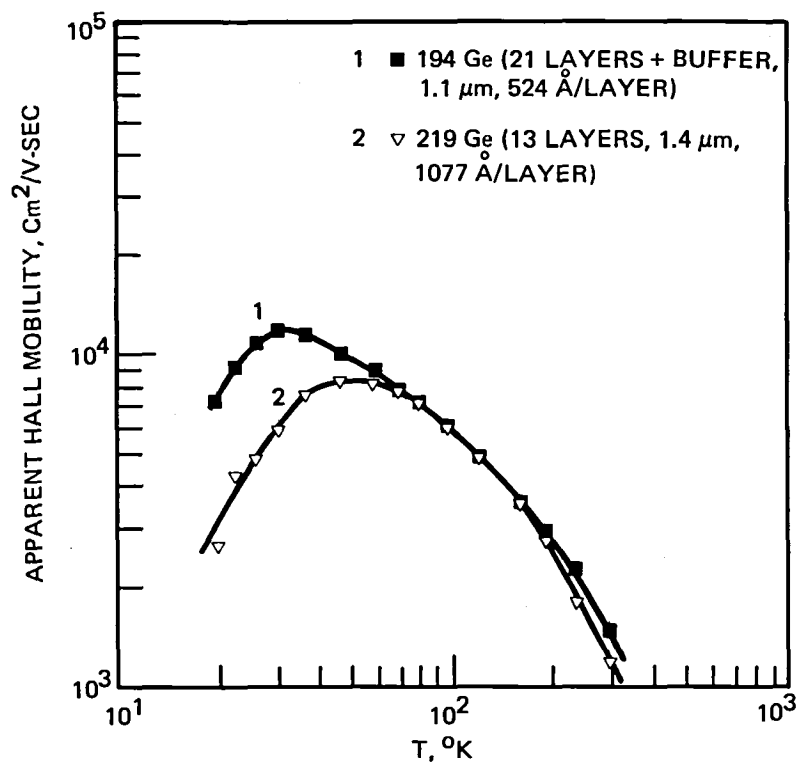


Figure 24. Comparison of Temperature Dependence of Hall Mobility for Multilayer Si/SiGe Samples with (No. 194 Ge) and without (No. 219 Ge) Buffer Layer.

An experiment was thus made to determine the carrier concentration as a function of depth using a capacitance-voltage measurement on a reverse biased Schottky or p⁺ junction made on the n-type semiconductor. The principle of the profiling is as follows:

The capacitance obtained in the C-V measurement is:

$$C = \frac{dQ}{dV} = \frac{dQ}{dW} \bigg/ \frac{dV}{dW}$$

Where dQ is the charge stored in the semiconductor layer of width dW and dV is the change in the applied voltage resulting in depletion layer width change dW, using the relations

$$C = \frac{A\epsilon}{W} \quad \text{and} \quad \frac{dQ}{dW} = Aq n(w)$$

where A is capacitor area, w is total depletion width, ϵ = Si or SiGe permittivity, q = electronic charge, and n(w) is the carrier density which is a function of w, we can write

$$\frac{d}{dV} \left(\frac{1}{C} \right) = \frac{d}{dW} \left(\frac{1}{C} \right) \bigg/ \frac{dV}{dW} = \frac{d}{dW} \left(\frac{W}{A\epsilon} \right) \bigg/ \frac{Aqn(w)}{C} \quad \text{or} \quad \frac{d}{dV} \left(\frac{1}{C} \right) = \frac{C}{A^2 q \epsilon n(w)}$$

Thus n(w) can be determined knowing both $\frac{1}{C}$ and its derivative with respect to the bias voltage.

Now the value of n(W) obtained here is not equal to the free carrier concentration; rather it is equal to the free charge carrier density plus the change in the charges on the impurities and trapping sites in response to the change of the applied voltage. At high temperature where the donors are completely ionized, n then becomes equal to the free electron concentration. At low temperature where carrier freezeout is expected to occur, the interpretation of quantity n(W) becomes quite complicated since the charge contribution from the donors occurs at different locations from the edge of the depletion layer (the Fermi level crosses the donor levels at finite distance away from the depletion layer edge). At any rate n(W) sets an upper limit on the value of the actual free carrier concentration. In the following n(W) will sometimes be referred to as the carrier concentration, however it is important to keep the above definition in mind.

Measurements were first made using the Leighton Electronics Miller Feedback Profile Plotter Model 2000. Later measurements were made on a computerized set up using a Hewlett-Packard Impedance Analyzer Model 4192A for direct measurement of the capacitance as a function of voltage.

Schottky diodes were fabricated on several films, some had Cr-Au and some had MoSi₂ metallization. The results are shown in Figures 25, 26 and 27 respectively. The measurement is limited from below by the depth of the depletion layer at zero bias and from above by the junction breakdown. At room temperature, n was modulated substantially with the peak to valley ratio of 2.0 or more. The period of the carrier modulation coincided with that of the film (period = Si + SiGe thickness).

It was first thought that the maxima and minima corresponded to the SiGe or Si layer which have different doping when grown separately. This conjecture, however, turned out to be incorrect due to several factors. One of them is the observation that the peaks become extremely sharp at

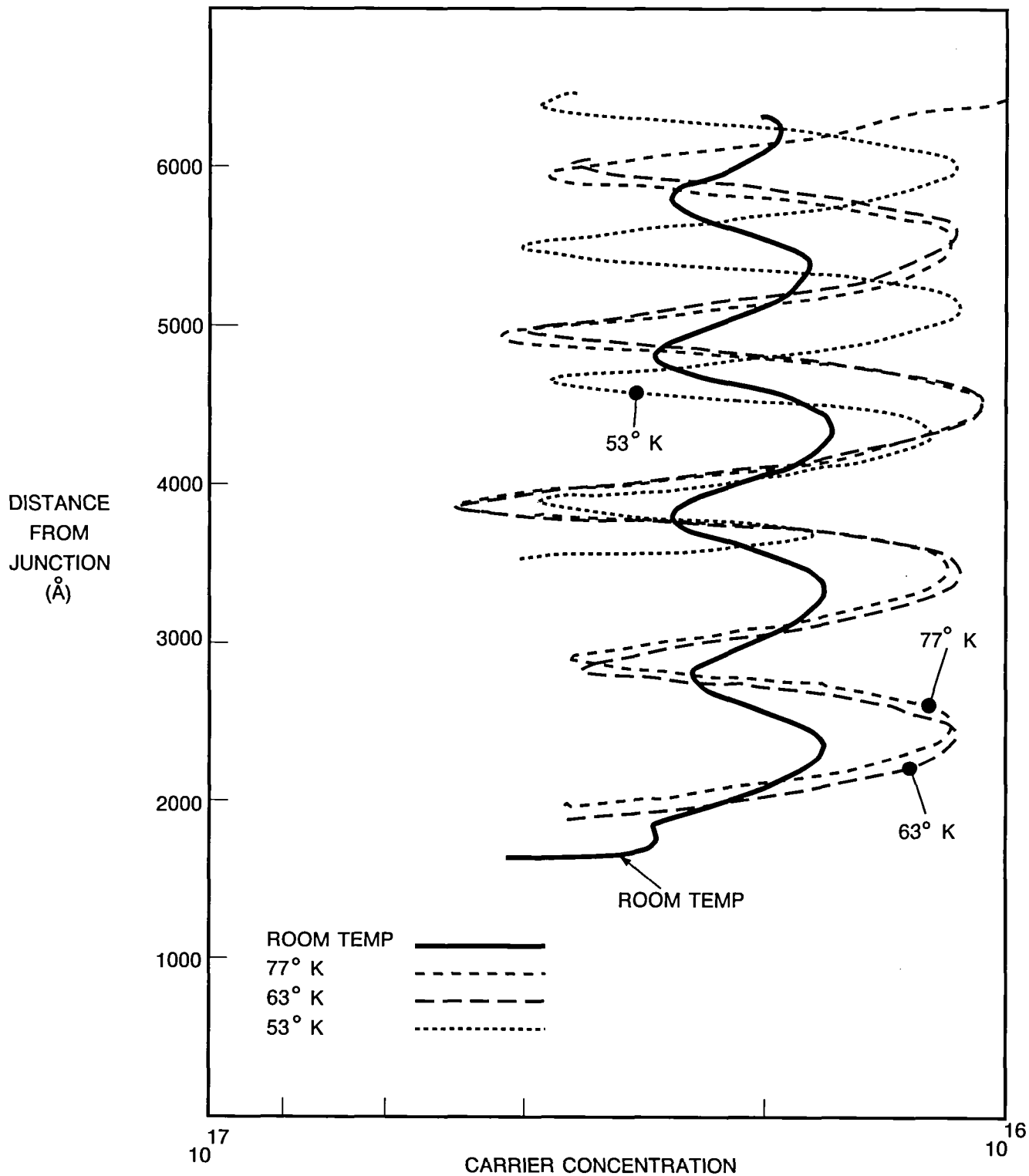


Figure 25. Carrier Concentration Profile of Sample No. 29

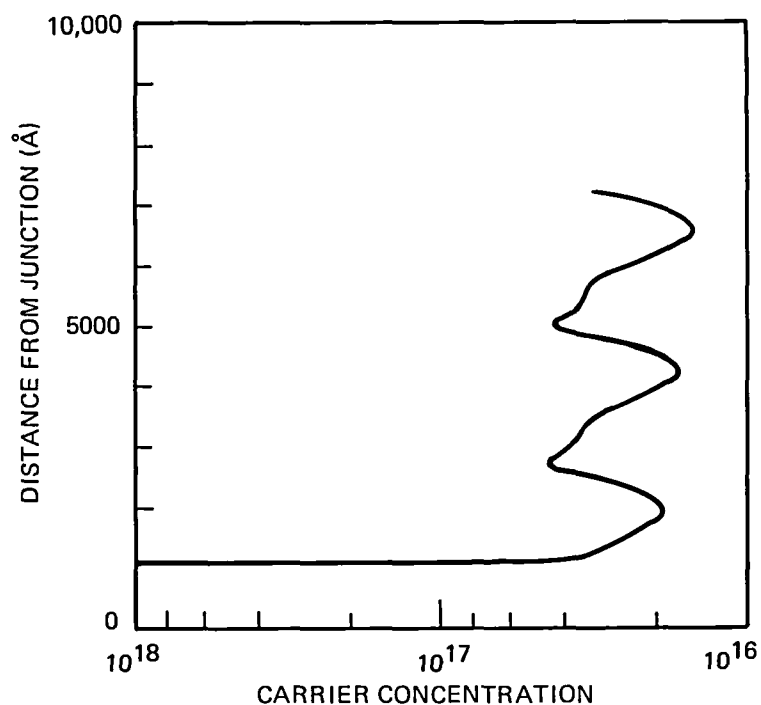


Figure 26. Carrier Concentration Profile of Sample 48 at Room Temperature

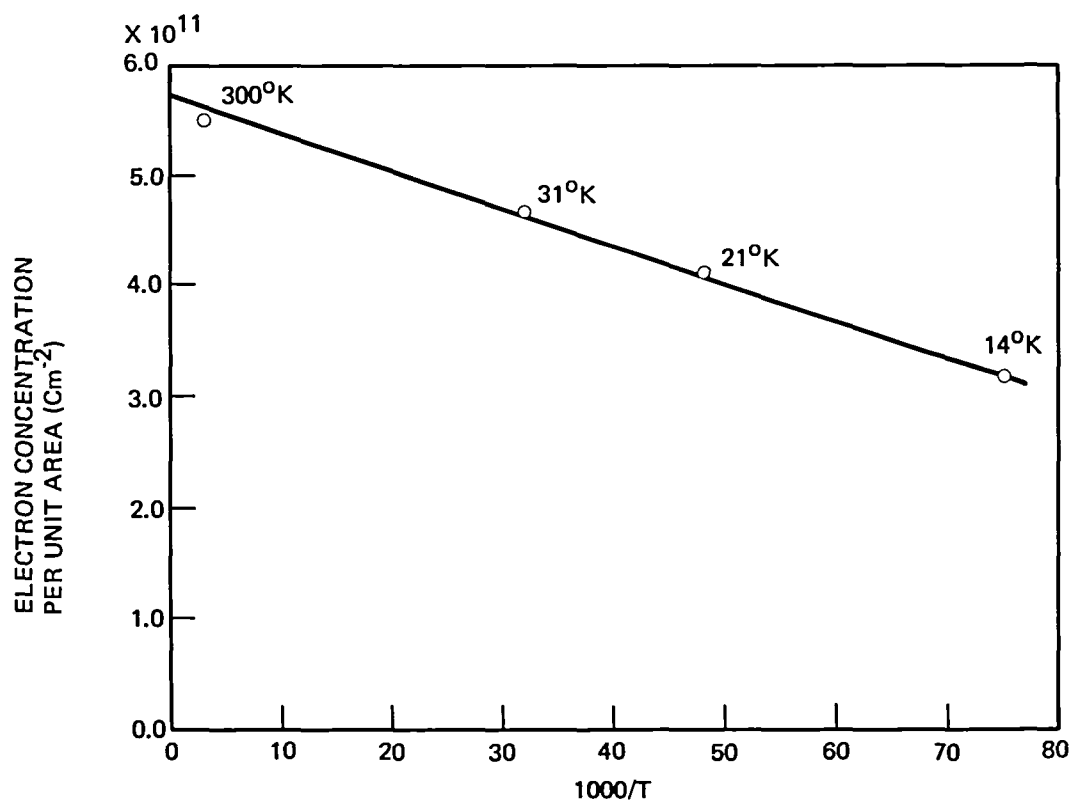


Figure 27. Total Number of Electrons Per Unit Area in a Super Lattice Period in Sample No. 48

low temperature as shown in Figure 28 and Figure 29 which shows the evolution of the n distribution as the temperature is lowered. This observation indicates that the peaks occur at well defined planes in the film which are most likely the interfaces between layers. Assuming that to be the case, by matching the profile of n to the known layer sequence of the film using the surface as a reference point, the peaks were identified with the SiGe on Si interfaces. The alternate interfaces i.e., Si on SiGe, do not seem to correspond to any particular feature in the carrier profile.

At this point we considered two possibilities to account for these observations. The first is the transfer of electrons across the heterojunction mentioned earlier. The second possibility is the following: the Si and SiGe layers have fairly large mismatch in both their lattice parameters and thermal expansion coefficients. These are expected to cause large numbers of defects at the layer interface and also in the bulk of the epitaxial layers. The defects can act as gettering centers for impurity atoms resulting in dopant segregation to the interfaces. At higher temperature the carrier distribution is relatively broad due to thermal diffusion of carriers away from the dopant atoms (Debye screening), and at lower temperature the distribution becomes narrower and more peaked.

The next step in this investigation was the measurement of drift and Hall mobility profiles to see if it could shed more light on the problem of determining the electronic structure of our films. The measurements are made using gated Hall devices (GHD) whose fabrication procedure is presented in detail in the next chapter. The device is basically a Schottky junction field effect transistor whose structure is shown schematically in Figure 30. All the pads except the gate have ohmic contacts. The gate (Pt silicide) covers the channel area and extends over to one pad (No. 6). Pads 1 and 5 are connected to the voltage (or current) supply. The voltage drop along the channel is measured between pads 2 and 4 (or 2 and 3). The Hall voltage across the channel is measured between pads 3 and 7.

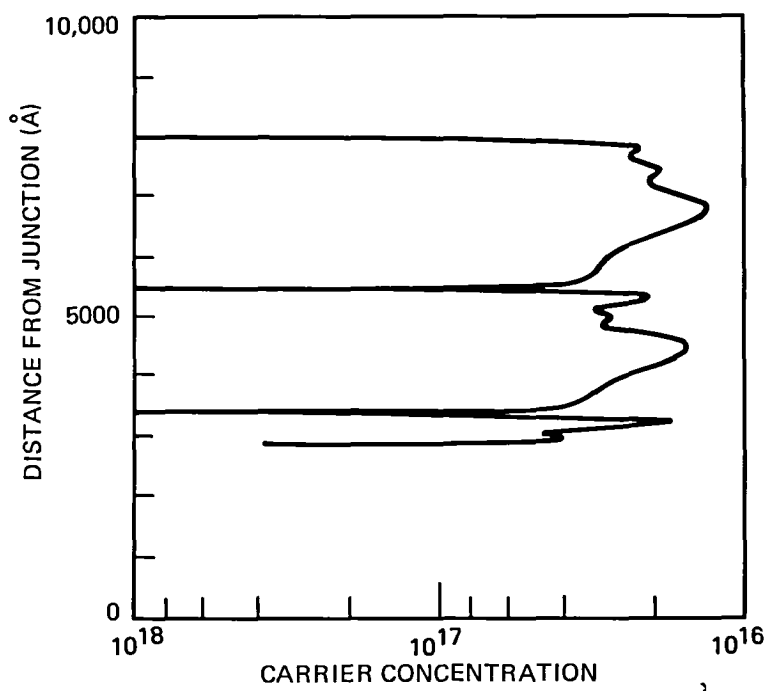


Figure 28. Carrier Concentration Profile of Sample 48 at 31°K

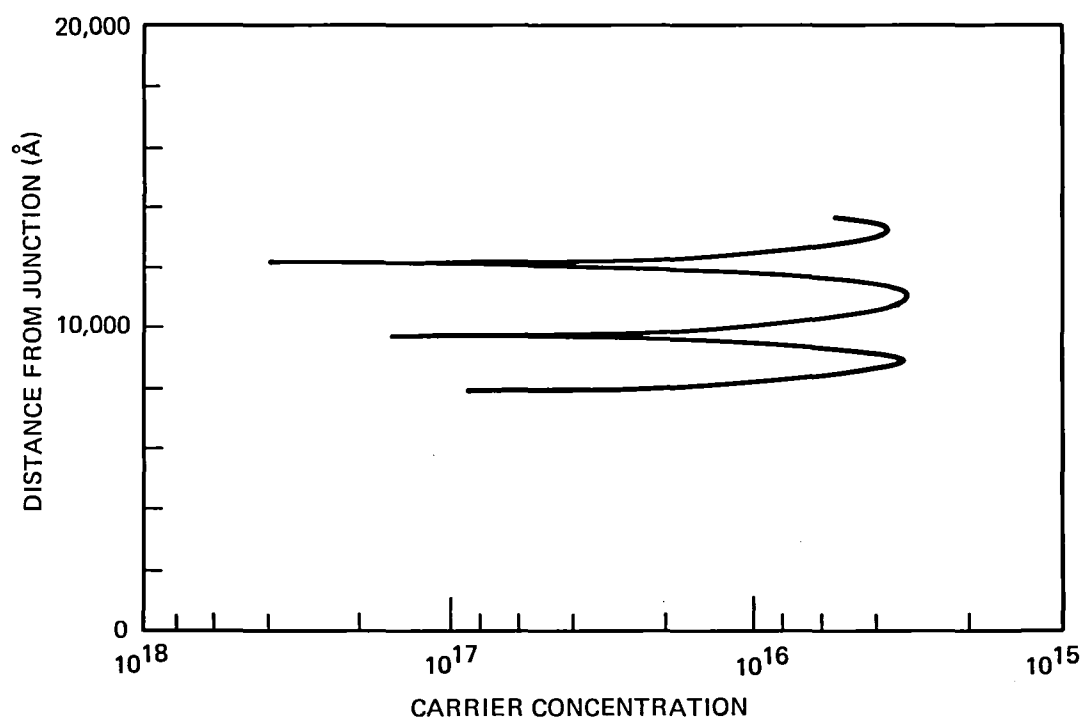


Figure 29. Carrier Concentration Profile of Sample No. 48 at 21°K

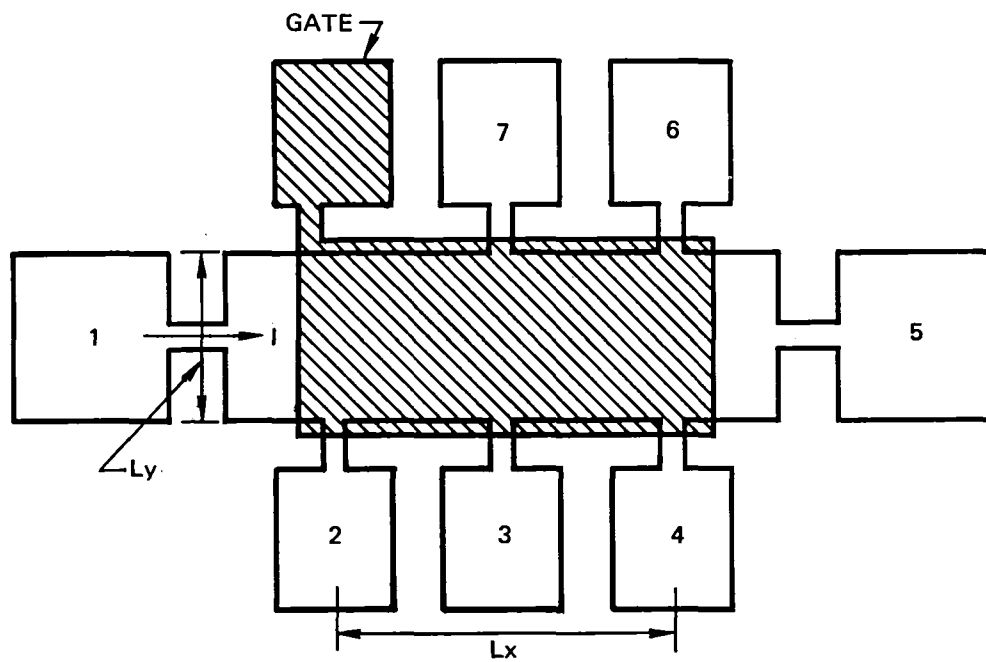


Figure 30. Gated Hall Device

The measurement of the drift mobility is made as follows: a voltage supply is connected to pads 1 and 5 and the current (I) is adjusted such that the voltage drop between pads 2 and 4 is small enough not to affect the depth resolution of the measurement. For example, in our case

$n \sim 10^{16} \text{cm}^{-3}$, and the built-in voltage $\sim 0.8 \text{eV}$ at $V_g = 0$, $\frac{\Delta W}{\Delta V_g} = \sqrt{\frac{q}{2 \epsilon N V_{bi} V_g}} \sim 2000 \text{ \AA/volt}$ or a

depth resolution of $\sim 200 \text{ \AA}$ for $V_{14} = 0.1 \text{ volt}$. At larger V_g the depth resolution improves further. The channel conductance at a given gate voltage is given by:

$$G = \frac{q L_y}{L_x} \cdot \int_w^h \mu(z) n(z) dz, \quad (1)$$

where h is the total film thickness and w is the depletion width given by the equation:

$$V_g + V_{bi} = \frac{q}{\epsilon} \int_0^w z n(z) dz, \quad (2)$$

Differentiating (Eq 1) and (Eq 2) w.r.t. W we get

$$\begin{aligned} \frac{dG}{dW} &= -q \frac{L_y}{L_x} \mu(w) n(w), \text{ and} \\ \frac{dV_g}{dW} &= \frac{q}{\epsilon} w n(w) \end{aligned} \quad (3)$$

dividing (Eq 3) by (Eq 4)

$$\frac{dG}{dV_g} = - \frac{\epsilon L_y}{w L_x} \mu(V_g) = - \frac{L_y}{L_x} \mu(w) C(W) \quad (4)$$

where $C(W)$ is the junction capacitance per unit area as measured by C-Vg technique.

The channel conductance is determined from the I-V measurement and is equal to:

$$G = \frac{I_{15}}{V_{24}} \quad (5)$$

Thus from G-Vg and C-Vg measurement the value of μ as a function of gate voltage (or depth) is obtained. Now, since the quantity n measured by the C-V technique represents an upper limit for the free carrier density, the value of μ otherwise represents the lower limit for the actual drift mobility.

The Hall mobility profile can be extracted from the measurements of V_{37} , V_{24} as a function of gate voltage as follows; In a film where the mobility μ , the Hall factor V_H , and carrier density n vary with depth the equations governing the Hall measurement are given by:

$$J_x(z) = q \mu(z) n(z) E_x + q \mu^H(z) \mu(z) n(z) E_y B_z \quad (6)$$

$$J_y(z) = q \mu(z) n(z) E_y - q \mu^H(z) \mu(z) n(z) E_x B_z \quad (7)$$

where μ and μ^H are the drift and Hall mobilities respectively; their ratio μ^H/μ is the Hall factor R_H which, we assume, is also a function of z . Integrating (Eq 6) and (Eq 7) over z we get

$$J_x = q E_x \int \mu(z) n(z) dz + q E_y B_z \int \mu^H(z) \mu(z) n(z) dz \quad (8)$$

$$J_y = q E_y \int \mu(z) n(z) dz - q E_x B_z \int \mu^H(z) \mu(z) n(z) dz \quad (9)$$

where J_x and J_y are the sheet current densities.

Equating J_y with zero and substituting (Eq 9) in (Eq 8) we get neglecting the B^2 terms:

$$\frac{E_y}{E_x} = B_z \int \mu^H(z) \mu(z) n(z) dz / \int \mu(z) n(z) dz \quad (10)$$

$$\frac{J_x}{E_x} = q \int \mu(z) n(z) dz \quad (11)$$

Multiplying (Eq 10 and Eq 11) we get

$$\frac{J_x E_y}{E_x^2} = q B_z \int_w^h \mu^H(z) \mu(z) n(z) dz \quad (12)$$

The above quality is a function of the gate voltage through its dependence on W , the depletion width. Multiplying by $\left(\frac{L_y}{L_x}\right)^2$ we define the quantity $Z(W)$

$$Z(W) = \frac{I_x V_{37}}{V_{24}^2} = q B_z \left(\frac{L_y}{L_x}\right)^2 \int_w^h \mu^H(z) \mu(z) n(z) dz \quad (13)$$

differentiating w.r.t. W we get

$$\frac{dZ}{dW} = -q B_z \left(\frac{L_y}{L_x}\right)^2 \mu^H(W) \mu(W) n(W) \quad (14)$$

combining Equations (14) and (3) we get

$$\frac{dZ}{dG} = \frac{dZ}{dV_g} / \frac{dG}{dV_g} = B_z \left(\frac{L_y}{L_x}\right) \mu^H(W) \quad (15)$$

or

$$\mu^H(V_g) = \frac{1}{B_z} \left(\frac{L_x}{L_y}\right) \frac{dZ}{dV_g} / \frac{dG}{dV_g} \quad (16)$$

Again the dependence of μ^H on V_g can be translated to a depth profile through the W - V_g relation obtained from C - V_g measurement.

Drift Mobility and Carrier Density Profiles (Results)

The gated Hall devices were diced and mounted on DIP packages. The packages were plugged into a socket mounted on the cold finger of the cryostat. Leads connected the socket to the instruments outside the cryostat unit. The source/drain and gate biases were supplied by the Hewlett-Packard 4140B digital picoammeter and voltage supply unit which also monitors the drain current. The voltage drop along the channel V_{24} was monitored by a Hewlett-Packard digital voltmeter Model 3455B. The instruments were interfaced with a microcomputer MINC (Digital Equipment Corp) which collected, processed and plotted the data as required.

Three devices were tested extensively in this experiment. The first device (No. 324) was fabricated on a $1\mu\text{m}$ multilayer film with 21 layers, the second device (No. 231) was fabricated on a relatively thick film ($\sim 4.3\mu\text{m}$) with 61 layers, and the third device (No. 315) was fabricated on a $1\mu\text{m}$ Si epitaxial layer.

The data obtained for the channel conductance (per square) of device No. 324 as a function of gate voltage is shown in Figure 31. The C - V_g measurement is shown in Figure 32. Both sets of data were taken at room temperature. The drift mobility and carrier density profiles extracted from these data are shown in Figure 33.

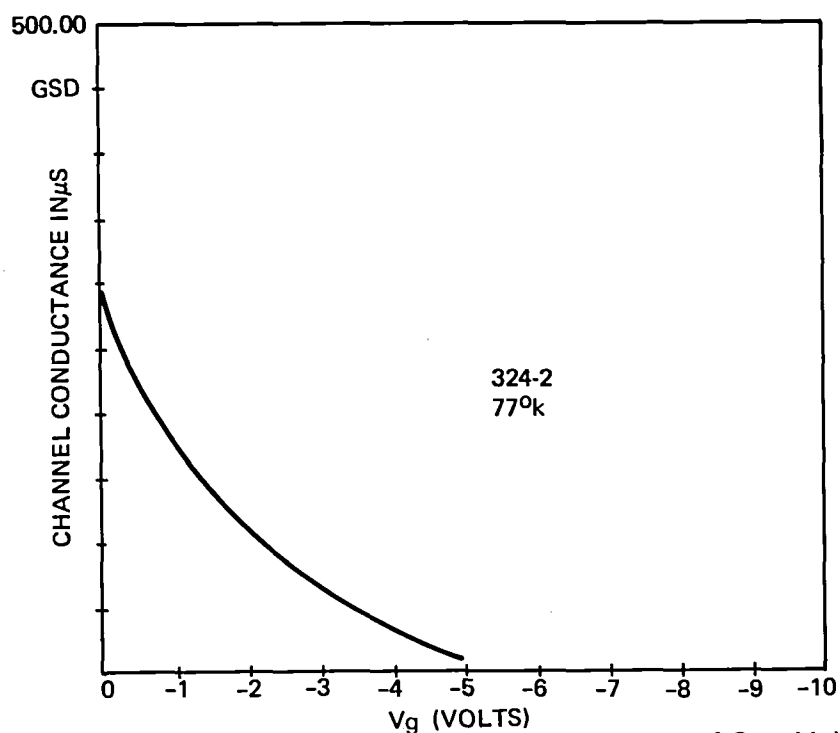


Figure 31. Channel Conductance of Device 324 as a Function of Gate Voltage at 77°K

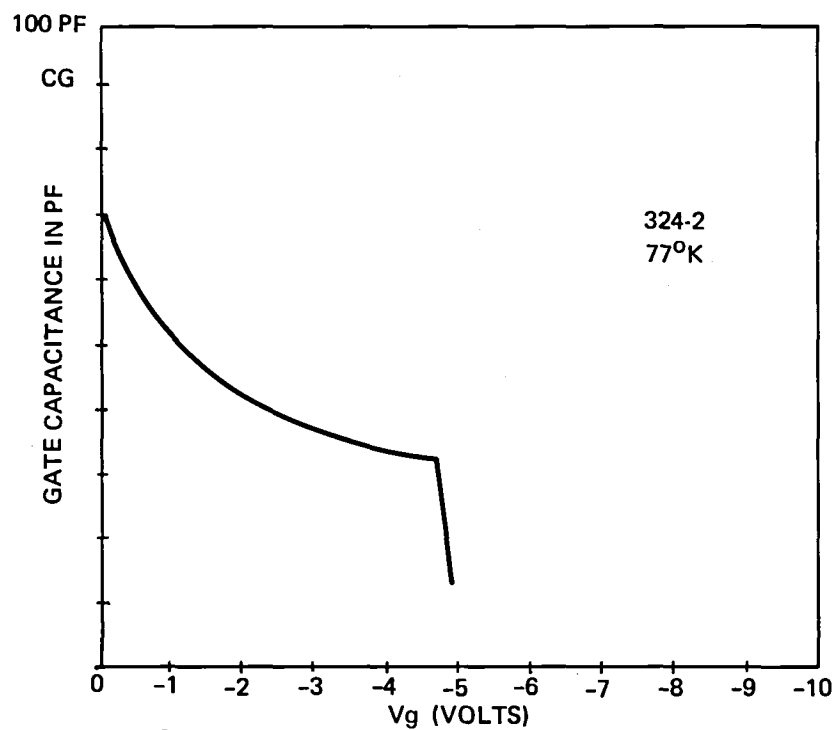


Figure 32. Gate Capacitance Versus Gate Voltage of Device 324 at 77 °K

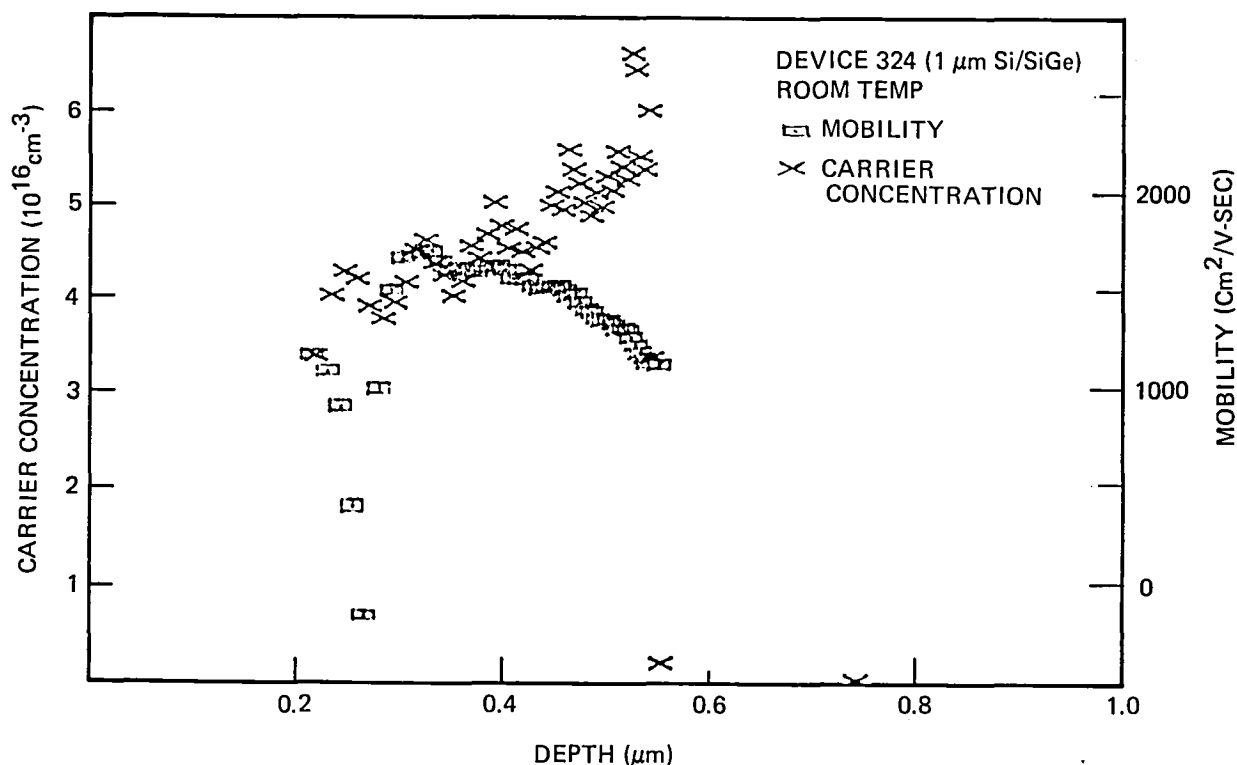


Figure 33. Carrier Concentration (X) and Drift Mobility (□) Profiles of Device 324 at Room Temperature

The modulation of n is quite discernable and the modulation period is about 950\AA which is close to the estimated value of $\sim 1000\text{\AA}$ based on the known growth rate of the film. The modulation of μ is hardly discernable. We notice, however, the steady drop of μ with depth. The results of the measurement at 77°K are shown in Figure 34. Here the modulation in n is much stronger than at room temperature. The modulation of μ is now very clear. Two important features are apparent. The first is that the peak in μ is very close to that of n which has important implications in the interpretation of the results in terms of the electronic structure of the films as will be discussed in Section 6. The second feature is that the value of μ apart from the modulation also drops sharply with depth as seen also at room temperature. This feature concurs with the previous observation that thin multilayer films ($< 1\mu\text{m}$) exhibit low Hall mobility since the measurements give an average mobility with depth and are thus a reflection of unevenness of the layers near the substrate interface which was seen in the TEM examination of the multilayer films.

The thicker device (No. 231) measurement is considerably more interesting since it shows the film properties away from the substrate interface. As seen in Figure 35 the modulation of n and μ are both clear at room temperature and again their peaks almost coincide. Figures 36 and 37 show the evolution of n and μ as temperature is lowered to 77°K and 31°K respectively. The peaks of n and μ become increasingly sharp as the temperature is lowered. We should point out that although n is a local property its measurement resolution is limited by thermal diffusion (Debye screening) and thus improves as the temperature is lowered. The data show a peak half-width of $< 100\text{\AA}$ at 33°K . On the other hand, the mobility is not a local property and can only be defined within a distance of several times the electron mean free path. The data at 31°K however

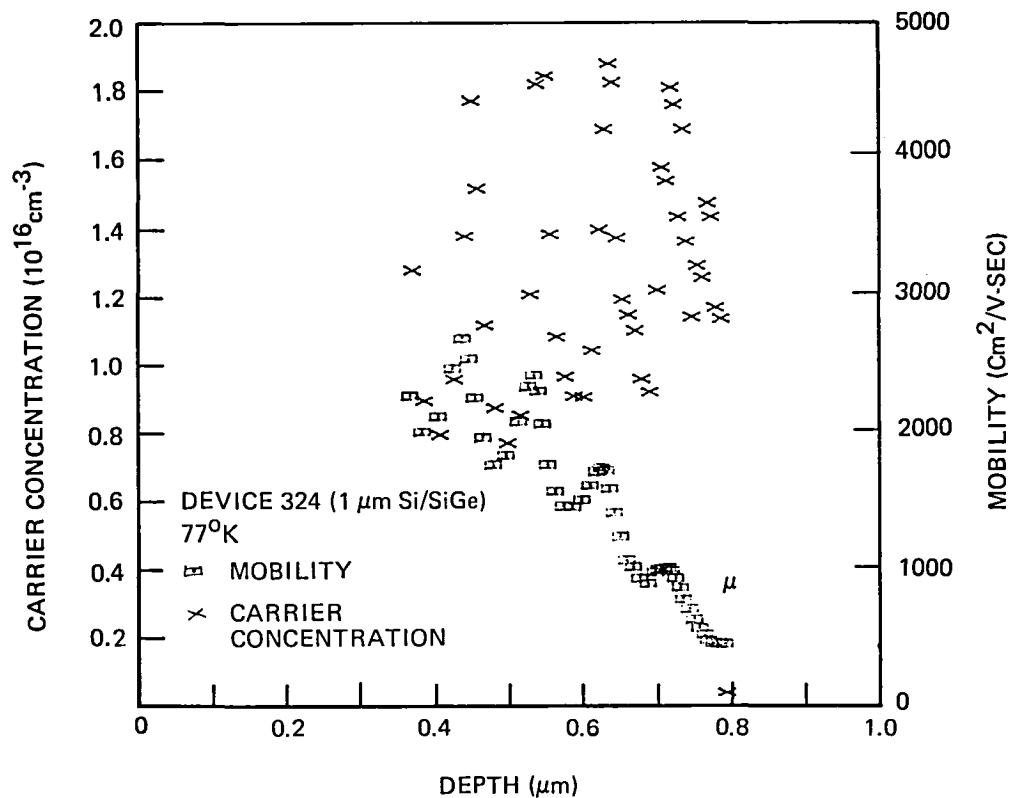


Figure 34. Carrier Concentration (X) and Drift Mobility (□) Profiles in Film No. 324 at 77°K

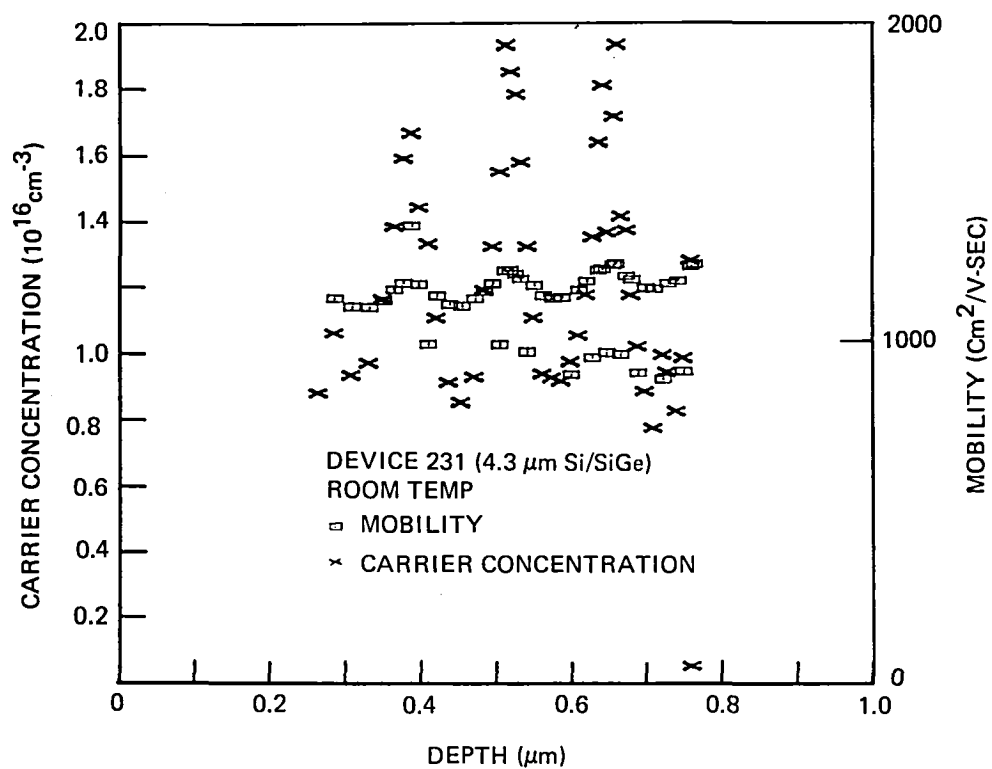


Figure 35. Carrier Concentration (X) and Drift Mobility (□) Profiles in Device 231 at Room Temperature

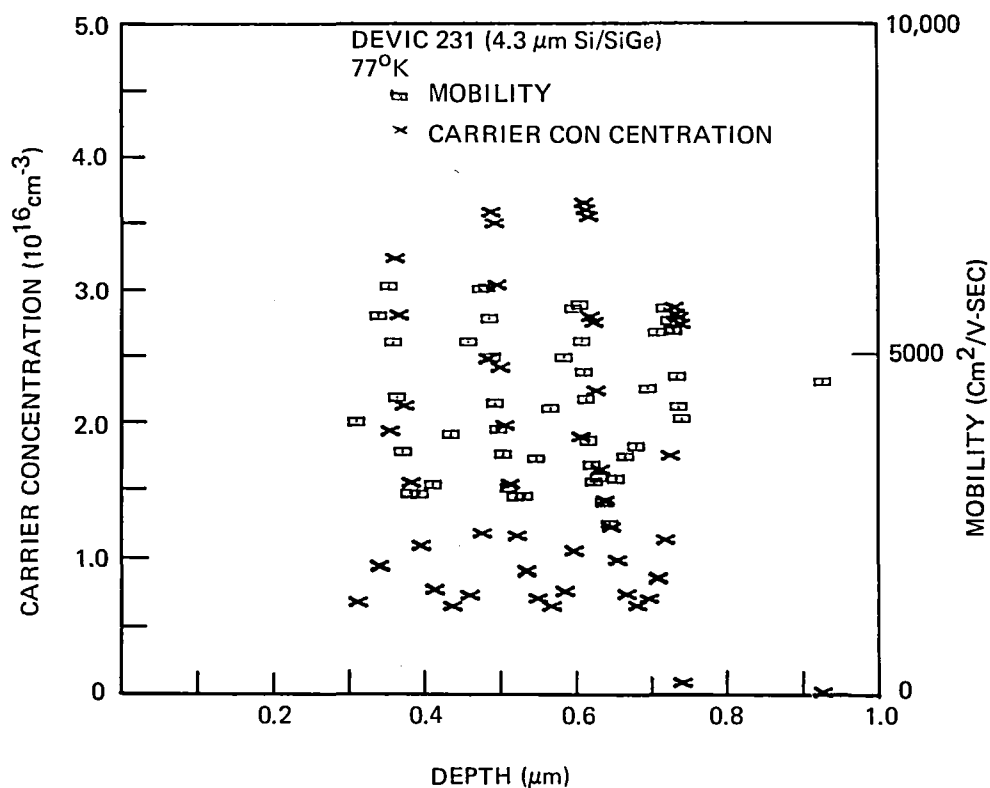


Figure 36. Carrier Concentration (X) and Drift Mobility (□) Profiles in Device 231 at 77°K

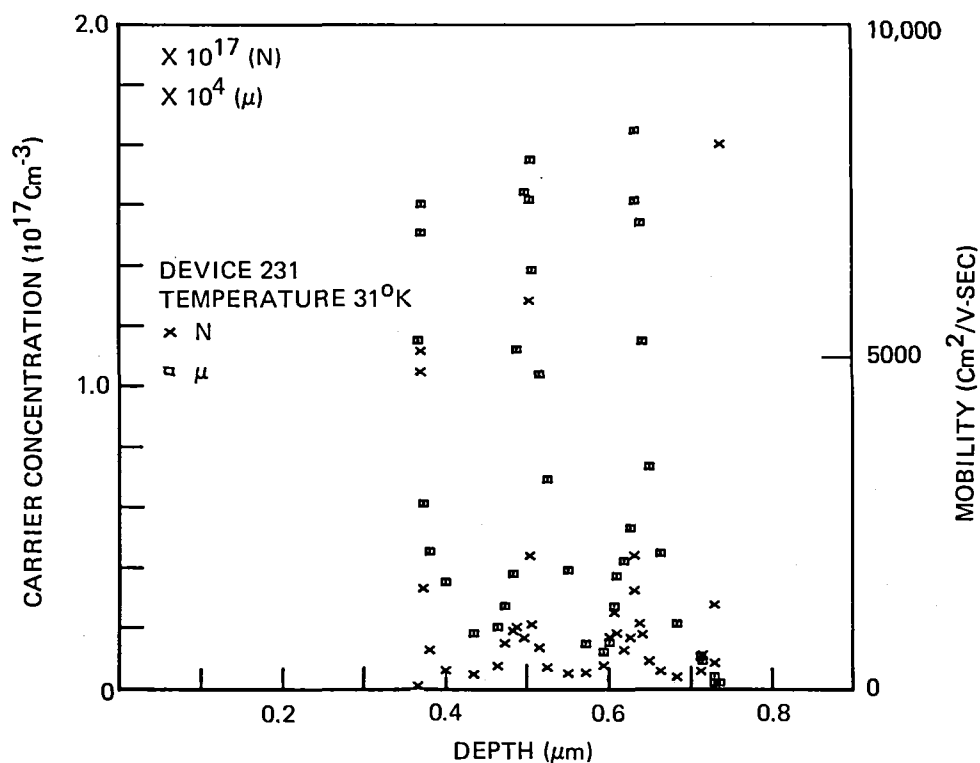


Figure 37. Carrier Concentration (X) and Mobility (□) Profiles of Film 231 at 30°K

show the peak half-width of μ to be about 200Å. An estimate of the value of $\mu \sim 10,000$ cm²/volt-sec in Si gives a half-width of about 1200Å at 30°K. This observation can be reconciled with the experimental results if we assume large anisotropic mobility or (more likely) if electrons are confined in a energy well of dimensions less than the peak width of μ . The peak value of μ is seen to reach 20,000 cm²/volt-sec at 31°K.

Hall Mobility Profile (Results)

The measurement of the Hall mobility profile is prone to errors for several reasons. Firstly, the Hall voltage is itself considerably smaller than the voltage drop along the channel for the magnetic field available (5000 gauss) by a factor of 1/20 (for $\mu \sim 1000$ cm²/volt-sec). Secondly, the time required for collecting the data is considerably larger than that of measuring the channel conductivity, since for each data point the magnetic field is reversed two times and allowed to stabilize for a few seconds. The result is higher chance of drifting in the measurements and more scatter in the results since the extraction of the values of μ^H involves taking differences between points. Typical results of the Hall mobility profile are shown in Figure 38 of sample No. 231 at 80°K. Here we can see the relatively large scatter in the data, however the modulation of μ^H with depth is visible. A program was written to smooth the data by recalculating each data point in terms of the values of its five neighboring points. The results recalculated are shown in Figure 39. The results show that the μ^H profile is very similar to that of the drift mobility in that the peaks of μ^H are very close to those of n . It also shows that μ^H is quite asymmetric in that its increase rate is much slower than its drop rate. Another feature is that the average mobility in the layers probed is considerably larger than that averaged over the whole film. For example, at room temperature the average μ^H over the whole film is about 1350 cm²/volt-sec. On the other hand, μ^H over the few layers being probed is between 1300 and 2000 cm²/volt-sec.

Summary

The highlights of the results reported in this chapter are:

1. Carrier non-freezout occurs in the multilayer films at low temperature.
2. The carrier concentration profile shows large peaks at low temperature where the nonfreezout occurs.
3. The electron mobility (both drift and Hall) is also modulated with depth. Mobility peaks almost coincide with those of the electron concentration. These peaks are identified with the alternate layer interfaces (SiGe on Si).

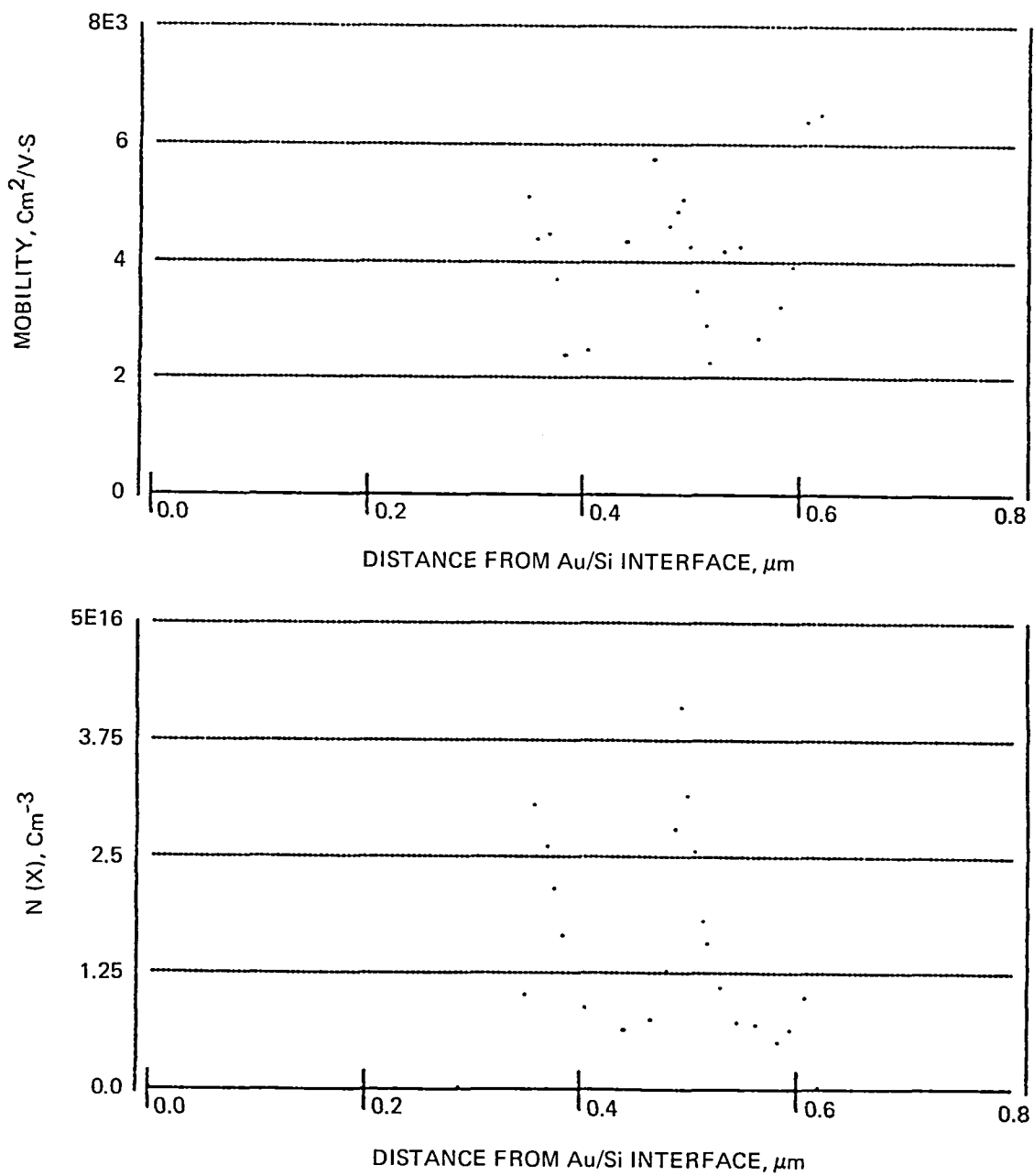


Figure 38. Hall Mobility and Carrier Concentration Profiles (Before Data Smoothing) of Device 231 at 80°K

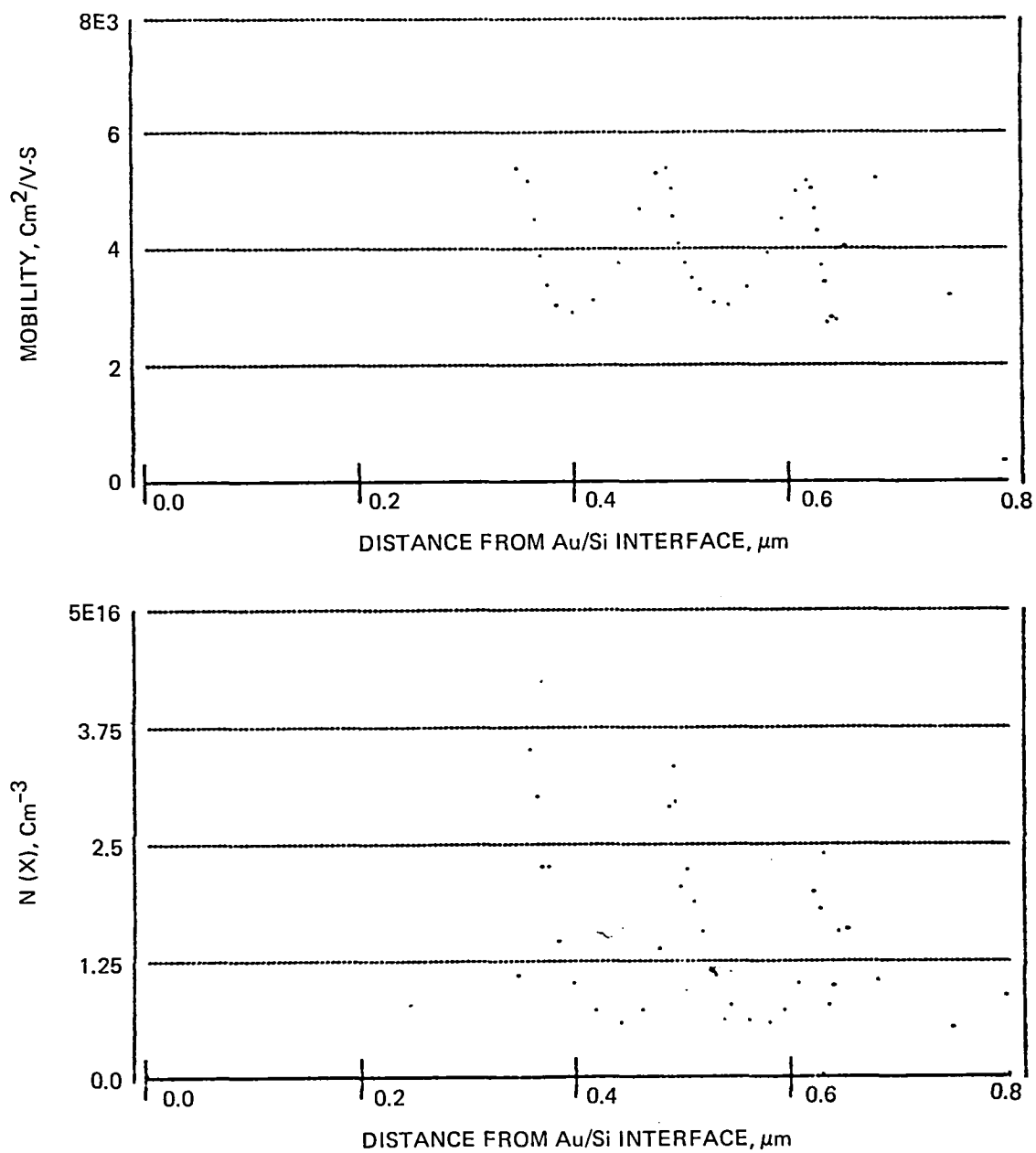


Figure 39. Hall Mobility and Carrier Concentration Profiles (After Data Smoothing) in Film No. 231 at 80°K

SECTION V

DEVICE FABRICATION

In this section we present the fabrication processes of the MESFET and MOSFET devices on multilayer Si/SiGe and single epitaxial Si layers on p-Si substrates, and the results of the device characterization. We also discuss the oxidation experiment performed on multilayer films and the results obtained in the characterization of the resulting oxide. Since the oxidation experiment chronologically preceded the FET fabrication we will start with the oxidation experiment.

Oxidation of Multilayer Si/Si_{1-x}Ge_x Films

The aim of this experiment was to evaluate the oxide grown on multilayer films. Both thin oxide (500-1000Å) for potential use as a gate insulator in MOS devices, and thick oxide (>2000Å) which could be suitable for device isolation (LOCOS) were examined. Two wafers were used in this experiment. One (No. 142) has three alternate layers starting and ending with Si layers of 500Å each sandwiching a 2000Å thick SiGe layer for a total epi thickness of ~3000Å. The second wafer (No. 136) had five layers (500Å Si alternating with 2000Å SiGe) for a total thickness of ~5500Å. The experiment was performed in two parts. The first part was to grow a thin oxide on the top Si layer of the wafer, which at about 500Å thickness should be sufficient to grow an oxide layer slightly thicker than 1000Å without consuming the underlying SiGe layer. The second part of the experiment was to grow oxide films of different thickness, starting with the same substrate, and to examine the product of the oxidation process.

Wafer No. 142 was oxidized at 875°C in wet O₂ for 60 minutes with the target SiO₂ thickness of about 1000Å. The oxidation was followed by annealing in dry N₂ for 30 minutes. The oxide thickness was 1040Å, measured with an ellipsometer. MOS capacitors were then fabricated on the wafer using the following procedure. A mask of 50 mil square dot pattern was applied and the oxide was etched outside the dots. Phosphorus implantation was made (80 keV, 1.2x10¹⁵cm⁻²) to form an n⁺ mesh to act as the return electrode for the epi layer. (The substrate is p⁻ and is thus not suitable for electrical connection to the n-type epi.) The photoresist was removed and the wafer was annealed at 875°C for 30 minutes, to activate the phosphorus implant. An aluminum film (~8000Å) was deposited over the wafer. A mask was applied with 25 mil dots inside the 50 mil oxide pattern and the aluminum was etched off outside the 25 mil dots. The wafer was sintered at 450°C for 15 minutes in forming gas.

The second experiment was to divide wafer No. 136 into four quadrants. Quads 1 and 2 were oxidized in steam at 875°C for 30 and 60 minutes, respectively. Quads 3 and 4 were also steam oxidized at 925°C for 68 and 300 minutes, respectively. The oxide thickness that should be obtained for Si under the above conditions are 500, 1000, 2000 and 5000Å, respectively.

The ellipsometric measurement of the oxides was successful only for the first two films. The last two films (Quads 3 and 4) gave readings that did not correspond to real solutions of a homogeneous dielectric over a Si substrate. The oxide thickness on Quads 1 and 2 were 540Å and 1015Å, respectively. The thickness of the oxides on Quads 3 and 4 was measured by etching a step and measuring the step height using a stylus profilometer. The steps were 2200 and 2500Å, respectively.

C-V Measurement of the MOS Capacitors and Voltage Breakdown of the Oxide

The C-V measurements were made at room temperature. The plot shown in Figure 40 is typical of what is obtained within the central portion of the wafer (~ 1 in. diameter). Outside the central part of the wafer, the plot was flatter, indicating lower doping level. The C-V data was fed into a computer program to calculate the interface state density and the results were tabulated in Table 7. The program was designed to handle uniformly doped semiconductors which was not the case for our film. However, for an order of magnitude estimate of the interface state density this seems like a reasonable choice. Here the density of interface states at the midgap is of the order of $10^{11} \text{ cm}^{-2}\text{V}^{-1}$, which is fairly reasonable for oxides grown in a steam atmosphere. Several MOS diodes were stressed for breakdown which occurred at about 50 volts, or about $5 \times 10^6 \text{ V/cm}$. A good thermal SiO_2 usually breaks down at about 10^7 V/cm .

Auger Analysis of the Oxide on Si/SiGe Films

The quadrants of Wafer 136 were analyzed using Auger spectroscopy in conjunction with ion milling to determine the composition as a function of depth. The procedure involves ion milling for a period of time then scanning the electron energy to determine the various elements present, then repeating the procedure over again. The results for Quad 1 to 4 are shown in Figures 41 through 44. Quads 1 and 2 show no trace of Ge in the oxide up to the semiconductor interface and a few hundred Å beyond. This is not surprising since only part of the uppermost Si layer is consumed during oxidation. For Quads 3 and 4 the oxide also does not show any Ge to within the sensitivity limit of the instrument which is only a few percent. However, a large Ge peak occurs at

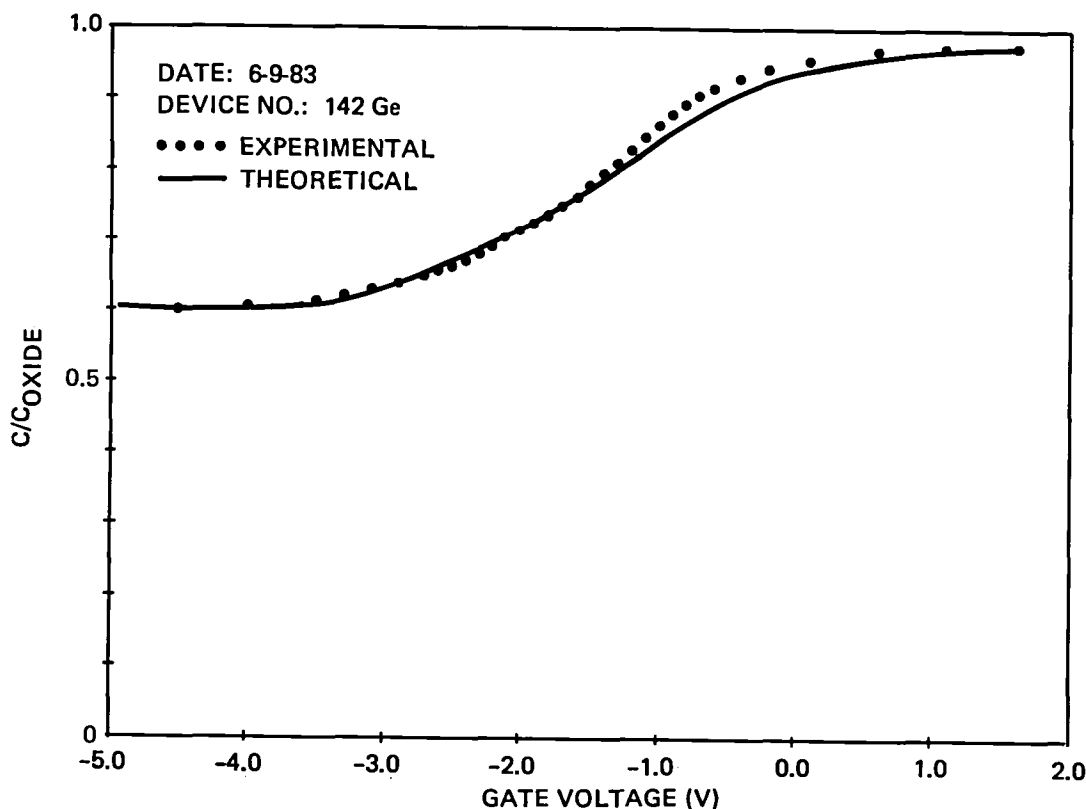


Figure 40. C-V Curve of MOS Capacitor in Sample No. 42

Table 7. C-V Measurements Data of Sample 124

<u>YG (Y)</u>	<u>C (PF)</u>	<u>US</u>	<u>CS (PF)</u>	<u>YG-YGFB (Y)</u>	<u>ES-EF (EY)</u>	<u>DF+DIT (NO./CM2)</u>	<u>DIT (NO./CM2EY)</u>
-5.0	78.7	-33.40	199.6	-4.94			
-4.5	78.7	-33.13	199.6	-4.44			
-4.0	78.9	-32.81	200.9	-3.94			
-3.5	79.9	-29.91	207.1	-3.44	-0.395	1.21E+10	
-3.3	80.8	-28.31	213.3	-3.26	-0.354	8.07E+09	9.84E+10
-3.1	82.0	-26.16	222.2	-3.10	-0.299	9.78E+08	1.28E+11
-2.9	83.4	-24.00	232.4	-2.94	-0.243	-8.38E+09	1.69E+11
-2.7	85.0	-21.56	245.5	-2.76	-0.181	-1.30E+10	7.37E+10
-2.6	85.9	-20.44	252.8	-2.68	-0.152	-1.62E+10	1.12E+11
-2.5	86.8	-19.17	261.4	-2.58	-0.119	-1.70E+10	2.27E+10
-2.4	88.1	-17.67	272.9	-2.47	-0.081	-1.35E+10	-8.97E+10
-2.3	89.4	-16.22	285.8	-2.35	-0.043	-1.01E+10	-9.15E+10
-2.2	90.8	-14.67	301.1	-2.22	-0.004	-4.29E+09	-1.46E+11
-2.1	92.1	-13.41	316.3	-2.11	0.029	-2.44E+09	-5.70E+10
-2.0	93.4	-12.28	331.9	-2.01	0.058	-2.36E+09	-2.83E+09
-1.9	94.8	-11.16	349.4	-1.91	0.087	-1.54E+09	-2.84E+10
-1.8	96.2	-10.08	369.8	-1.80	0.114	-7.85E+08	-2.73E+10
-1.7	97.7	-9.00	393.5	-1.70	0.142	9.11E+08	-6.13E+10
-1.6	99.4	-7.95	422.5	-1.58	0.169	3.23E+09	-8.56E+10
-1.5	101.3	-6.89	458.2	-1.47	0.196	6.89E+09	-1.35E+11
-1.4	103.3	-5.86	503.4	-1.34	0.223	1.17E+10	-1.80E+11
-1.3	105.6	-4.86	562.0	-1.21	0.248	1.76E+10	-2.32E+11
-1.2	107.9	-3.94	635.6	-1.08	0.272	2.41E+10	-2.73E+11
-1.1	110.3	-3.11	725.6	-0.95	0.293	3.06E+10	-3.03E+11
-1.0	112.5	-2.36	837.2	-0.81	0.313	3.74E+10	-3.55E+11
-0.9	114.6	-1.70	968.5	-0.68	0.329	4.40E+10	-3.93E+11
-0.8	116.4	-1.16	1110.4	-0.56	0.343	4.88E+10	-3.44E+11
-0.7	118.0	-0.67	1275.4	-0.43	0.356	5.40E+10	-4.21E+11
-0.6	119.3	-0.25	1450.1	-0.31	0.367	5.88E+10	-4.36E+11
-0.4	121.4	0.43	1829.2	-0.07	0.384	6.62E+10	-4.23E+11
-0.2	122.8	0.95	2211.8	0.14	0.397	6.94E+10	-2.41E+11
0.1	124.3	1.56	2831.3	0.46	0.413	7.34E+10	-2.51E+11
0.6	125.7	2.24	3775.4	0.92	0.431	6.42E+10	5.27E+11
1.1	126.5	2.71	4633.8	1.31	0.443	4.25E+10	1.82E+12
1.6	127.0	3.03	5379.0	1.64	0.451	7.70E+09	4.17E+12

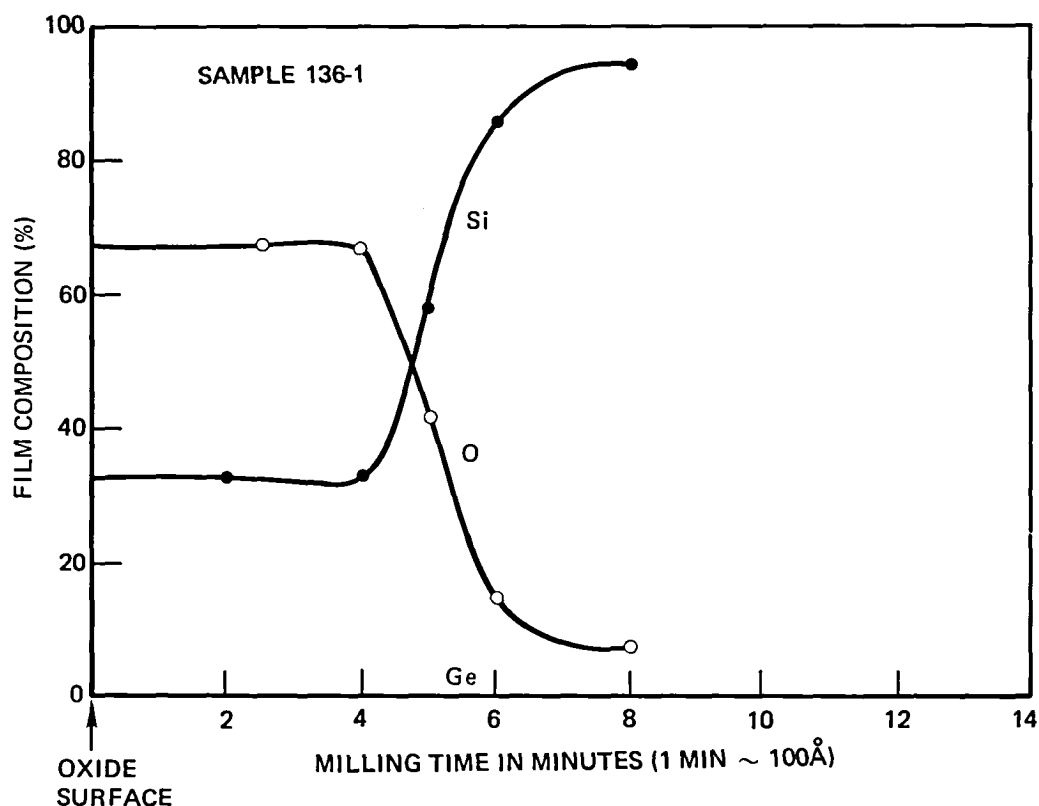


Figure 41. Auger Profile of Si, Ge, and O in the Oxidized Multilayer Film No. 136. (Oxidized in Steam for 30 Minutes at 875°C)

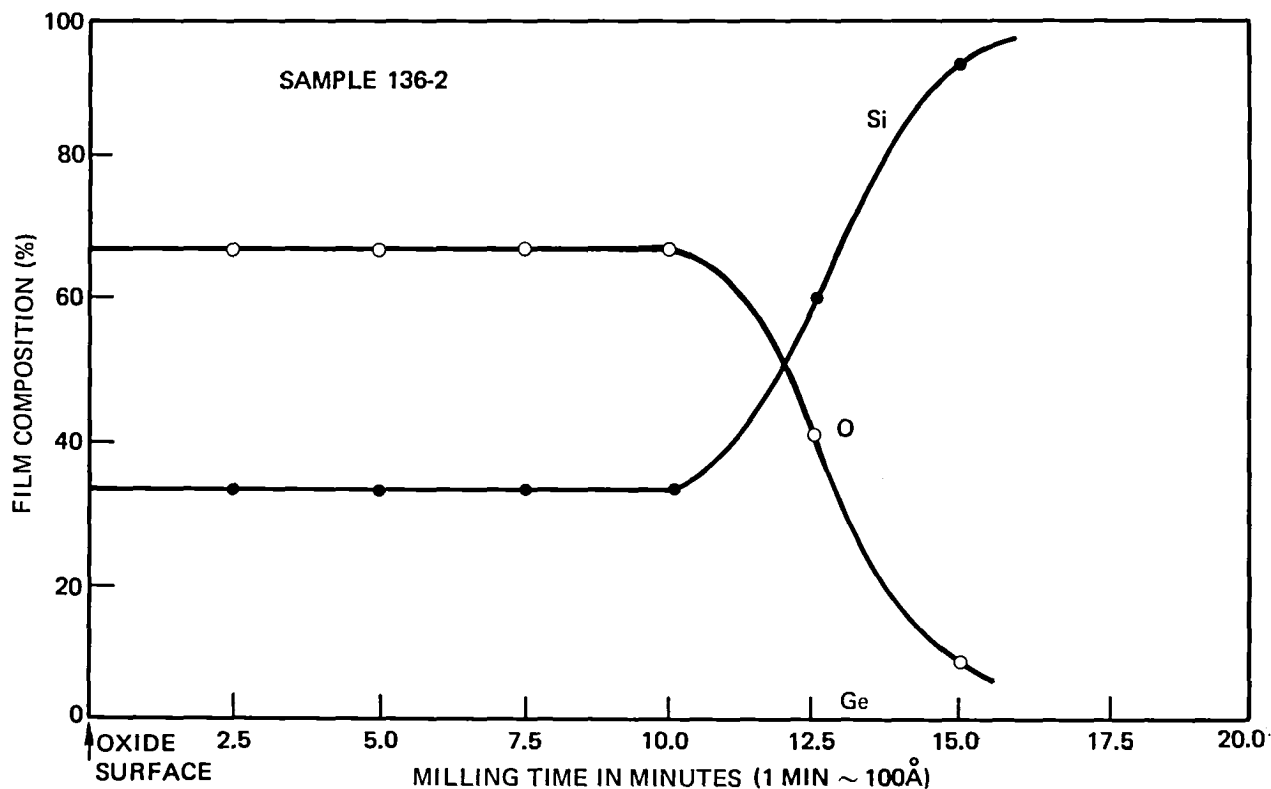


Figure 42. Auger Profile of Si, Ge, and O in the Oxidized Multilayer Film No. 136. (Oxidized in Steam for 60 Minutes at 875°C)

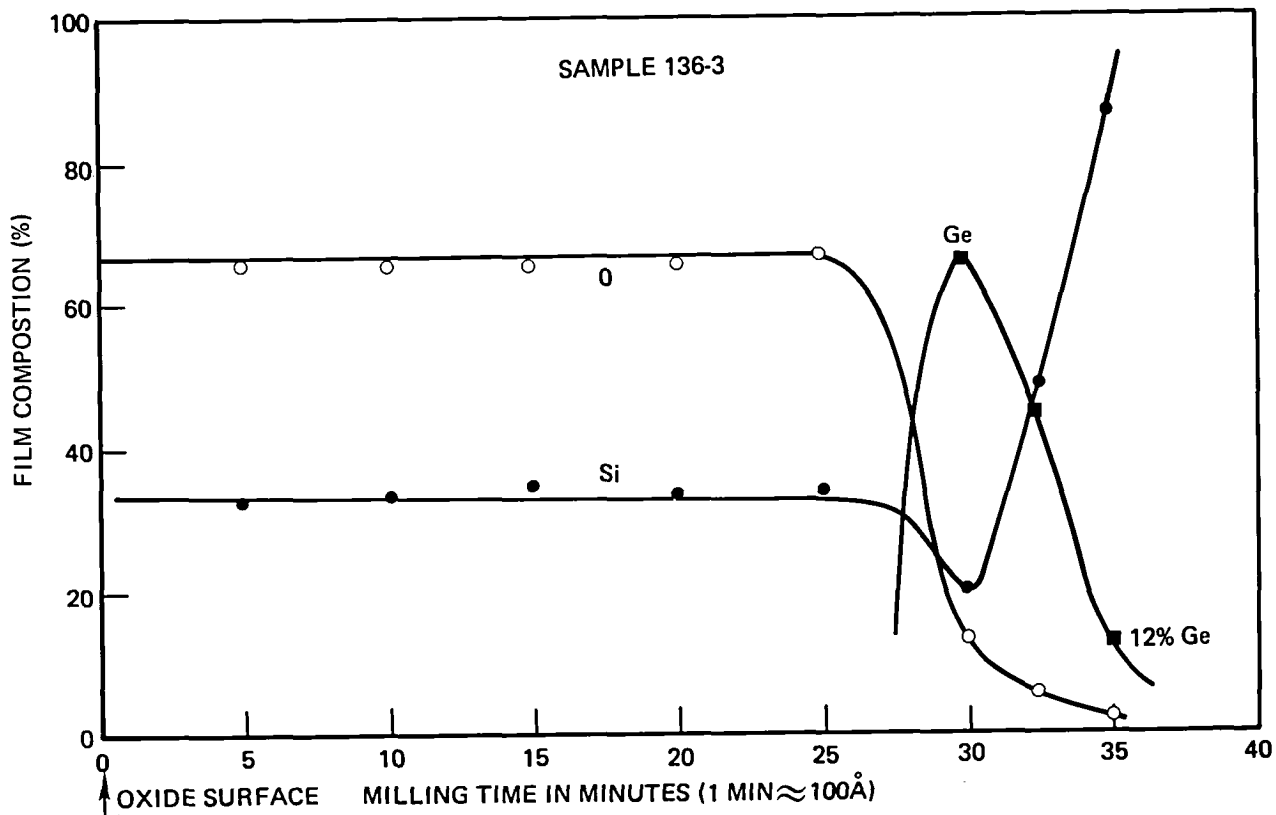


Figure 43. Auger Profile of Si, Ge, and O in the Oxidized Multilayer Film No. 136 (Oxidized in Steam for 68 Minutes at 925°C)

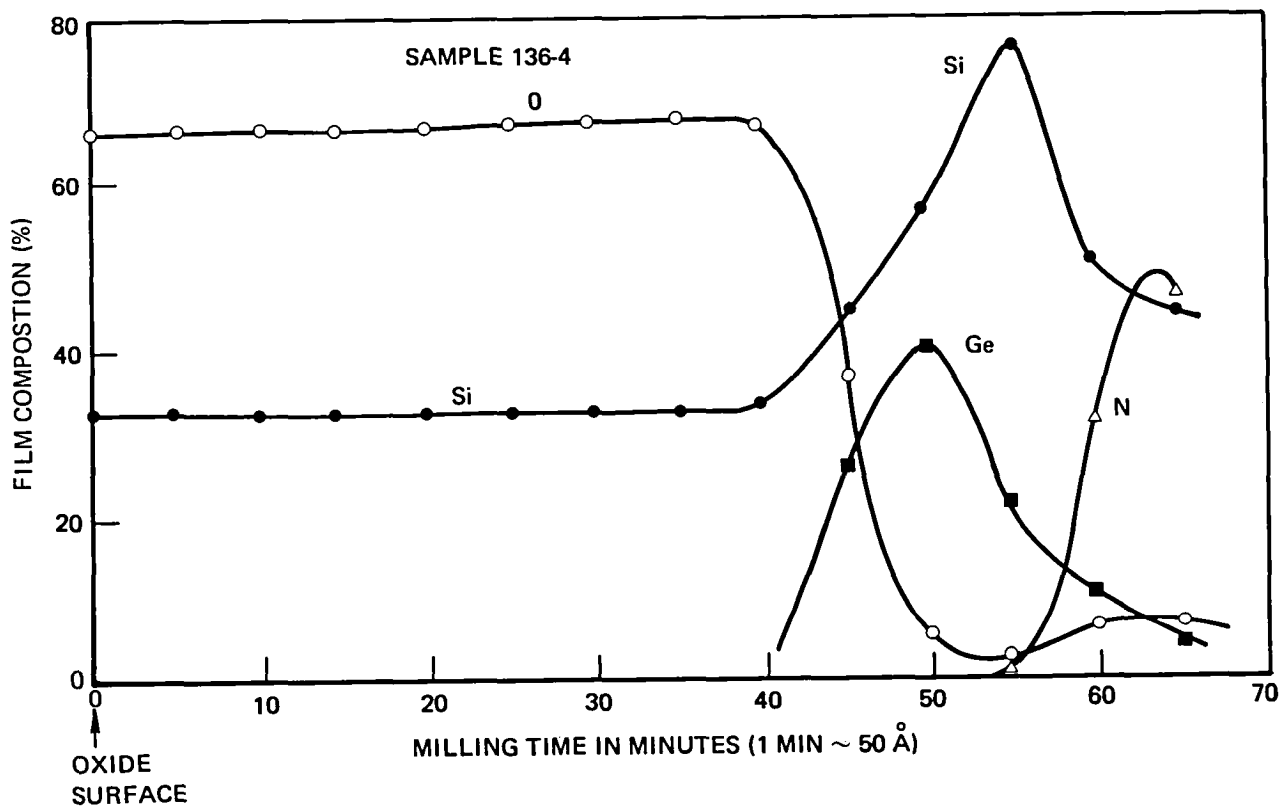


Figure 44. Auger Profile of Si, Ge, and O in the Oxidized Multilayer Film No. 136 (Oxidized in Steam for 300 Min at 925°C)

the oxide semi-conductor interface indicating pile-up of Ge at that interface. This result is in agreement with published data about the oxidation of SiGe alloys (Ref. 15). It is thus advisable to limit the oxidation of the multilayer films to the uppermost Si layer which should be of sufficient thickness for growth of the oxide. In cases where the required thickness of the uppermost Si layer is incompatible with the device structure, deposition of oxide might be useful.

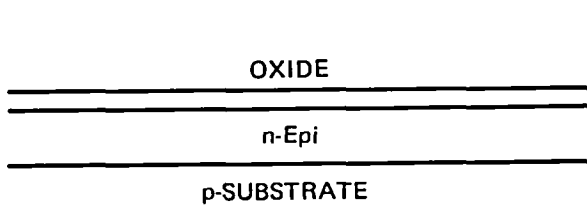
MESFET AND MOSFET DEVICE FABRICATION

The first device lot was based on an existing mask set designed originally for GaAs MESFETs. A process compatible with the mask design involves metal liftoff for the source/drain contacts and for the Schottky metal gates. This attempt was abandoned due to unsuccessful liftoff caused by poor adhesion of the metal to the semiconductor surface. A new mask set was designed and generated using an in-house electron beam exposure system (Cambridge EBMF). The mask set was designed for fabricating both MOSFET and MESFET devices using only five mask plates of which three are common for both devices. The processing steps, unlike the liftoff process, allow for rigorous cleaning to be performed before metal deposition. The device fabrication was successful on the first attempt and produced good working devices with characteristics close to those anticipated from the device design parameters and film properties.

The device lot contained 15 wafers: eight wafers with Si/SiGe multilayer epitaxial films, and seven wafers with n-Si epitaxial films. All epitaxial films were about $1.0\mu\text{m}$ thick. The nominal carrier concentrations in the Si/SiGe films were about $1.0 \times 10^{16} \text{cm}^{-3}$ and in the Si films were about $2.5 \times 10^{16} \text{cm}^{-3}$.

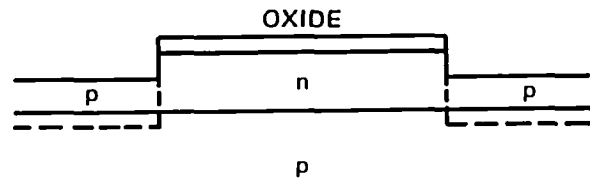
The 15 wafers went through the processing steps common to both the MOSFET and MESFET devices and then the lot was split into three groups: a group of four wafers (two SiGe and two Si) for MESFET device fabrication, four wafers (two SiGe and two Si) for MOSFET device fabrication, and seven wafers for backup. A step-by-step description of the fabrication procedure follows: (see also accompanying illustration in Figure 45.)

1. The wafers were first cleaned using the standard silicon acid cleaning procedure (sulphuric-peroxide, HF dip and hydrochloric-peroxide bath). The wafers were then loaded in the oxidation furnace. The oxidation cycle was 15 min. N_2 , 10 min. $\text{H}_2 + \text{O}_2$ and 20 min. N_2 , all at 875°C . The oxide thickness was measured using ellipsometry and was equal to $\sim 200\text{\AA}$. The oxide provided good surface adhesion for photoresist and also served to protect the semiconductor surface during the subsequent steps.
2. The wafers were coated with photoresist (1350J at 3000 rpm) which provided a $2.5\mu\text{m}$ thick layer. The photoresist was patterned to define the device area (Mask No. 1).
3. The oxide outside the device area was etched in buffered HF. The wafers were then loaded into a parallel-plate plasma etcher and about 5000\AA of the semiconductor was etched off using a $\text{CF}_4\text{-O}_2$ plasma.
4. The photoresist left on the wafers was measured and found to be of insufficient thickness for the next step, and thus the wafers were repatterned using the same device area mask used before (Mask No. 1)
5. Ion implantation of boron was made at 25, 70, and 160 keV each with a dosage of 2×10^{12} ions/ cm^2 . The last two steps, namely the etching of the top 5000\AA of the semiconductor and the boron implant, provided the device isolation to a depth exceeding the epi thickness.



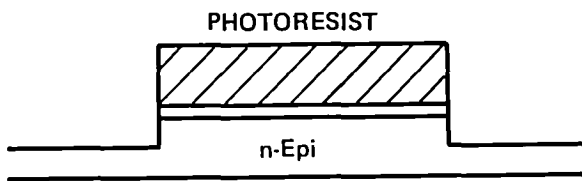
- THERMAL OXIDATION (500\AA) 925°C

— a —



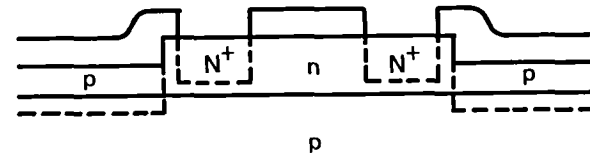
- ANNEAL AT 1000°C FOR 10 MIN TO ACTIVATE THE BORON IMPLANT

— d —



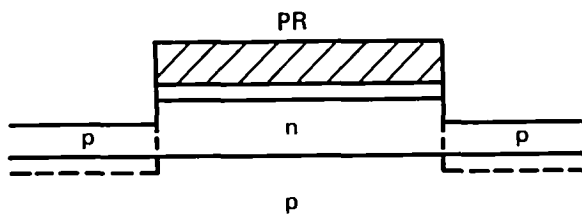
- APPLY ACTIVE AREA MASK
- ETCH OXIDE
- PLASMA ETCH $0.5\text{ }\mu\text{m}$ N Epi

— b —



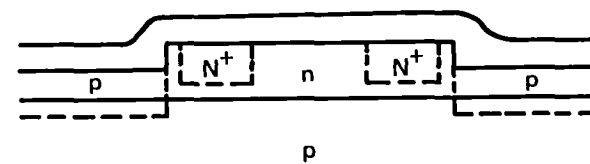
- ETCH OXIDE
- APPLY SOURCE/DRAIN MASK
- IMPLANT PHOSPHORUS $1 \times 10^{15}\text{ cm}^{-2}$ 60 AND 150 KeV

— e —



- IMPLANT BORON $2 \times 10^{15}\text{ cm}^{-2}$ AT 25, 70, 170 KeV

— c —



- DEPOSIT $5000\text{ }\text{\AA}$ LPCVD OXIDE AT 900°C (ALSO PHOSPHORUS ACTIVATION)

— f —

Figure 45. A to F: Processing Steps Common to Both MESFET and MOSFET Devices

6. The photoresist was removed in an oxygen plasma and the wafers were cleaned and then annealed in N_2 for 10 minutes at $1000^\circ C$ to activate the boron implant.
7. The wafers were coated with $2.5\mu m$ of resist and patterned with the source/drain implant mask (Mask No. 2). The phosphorus N^+ implant was done at 60 and 150 keV each with dosage = 10^{15} ions/cm². The photoresist was stripped in an oxygen plasma.
8. Field oxide was deposited in a low pressure CVD reactor by the reaction of SiH_2Cl_2 and N_2O_3 at $900^\circ C$. The deposition lasted 150 minutes and the oxide thickness was about 3000\AA . This step also activated the phosphorus implant in the N^+ source/drain region.

At this point the lot was split for the MESFET and MOSFET device fabrication.

MOSFET Fabrication

The following steps are illustrated in Figure 46.

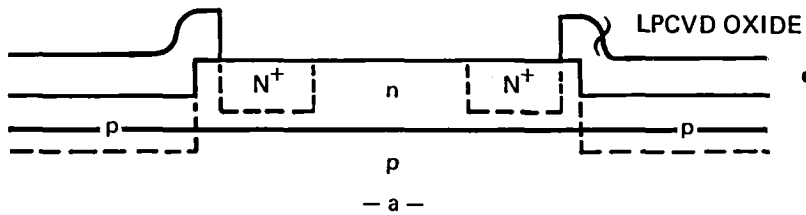
1. This step opens up the field oxide in the device active area. The wafers were masked (Mask No. 3) and the oxide was etched in buffered HF.
2. The wafers were cleaned and loaded in the furnace for the gate oxide growth. The growth cycle was 20 min in N_2 , 35 min. in $H_2 + O_2$ and 20 min in N_2 . The oxide was measured using a Nanospec instrument and was very close to 500\AA .
3. The wafers were patterned again with Mask No. 2 to open the gate oxide over the source drain region.
4. The wafers were cleaned and aluminum was deposited (8000\AA) to form the gate and contact metallization to the source/drain. The wafers were patterned with Mask No. 4 and the aluminum was etched and the photoresist was removed. The aluminum was then sintered by annealing the wafers at $450^\circ C$ in N_2 . This completes the MOSFET device fabrication.

MESFET Fabrication

The following steps are illustrated in Figure 47.

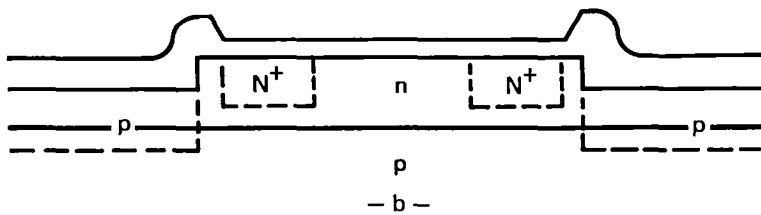
1. This step opens the field oxide over the source/drain and the gate area (Mask No. 5).
2. The wafers were loaded in a sputtering machine for the deposition of the Schottky gate metal (platinum). The wafers were first back-sputtered to clean their surface and then platinum was sputtered on them to a thickness of 300\AA .
3. The wafers were sintered at $450^\circ C$ for 20 minutes in forming gas ($N_2 + H_2$). The platinum film reacts with Si in the areas not covered with SiO_2 and forms $PtSi_2$.
4. The excess platinum over the field was etched off in warm ($45^\circ C$) aqua regia.
5. Aluminum was deposited on the wafers (8000\AA) and Mask No. 4 was applied and the aluminum was defined to form connections to the source/drain contacts and the Schottky gate.

This completes the MESFET device fabrication



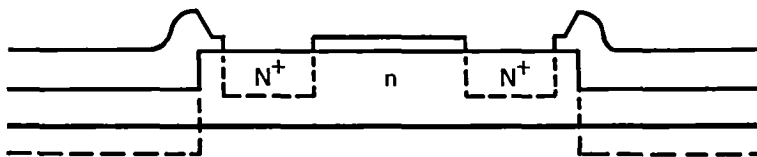
- ETCH OXIDE OVER DEVICE ACTIVE AREA

— a —



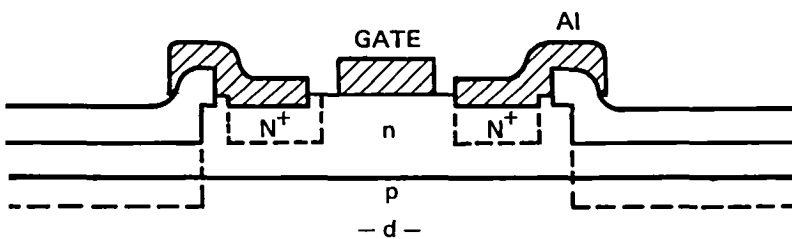
- GROW GATE OXIDE

— b —



- ETCH SOURCE/DRAIN CONTACTS IN GATE OXIDE

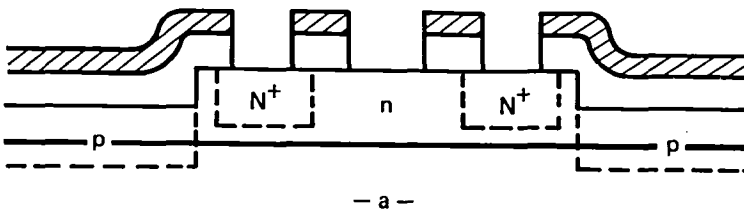
— c —



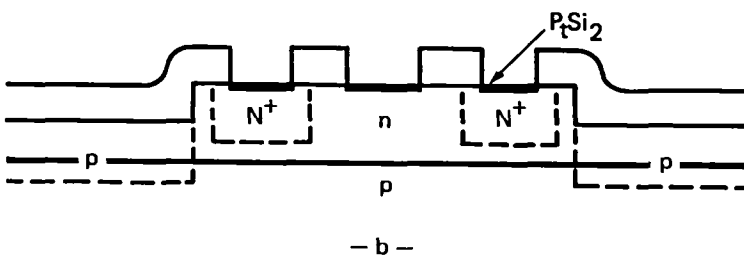
- DEPOSIT AND PATTERN ALUMINUM

— d —

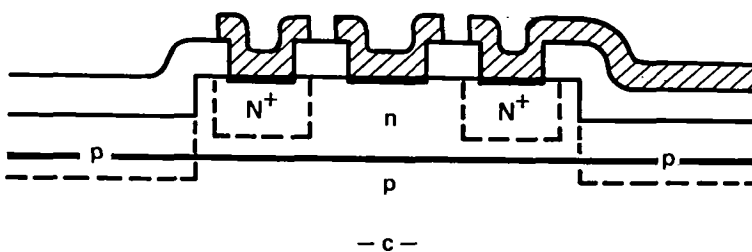
Figure 46. A to D MOSFET Processing Steps Following Steps in Figure 45



- APPLY GATE/CONTACT MASK
- ETCH OXIDE



- SPUTTER 300 Å Pt
- SINTER AT 450 °C FOR 20 MIN IN FORMING GAS
- ETCH EXCESS Pt IN WARM AQUA REGIA



- EVAPORATE 8000 Å Al
- APPLY METAL MASK
- ETCH Al

Figure 47. A to C Processing Steps for MESFET Devices (Following Steps in Figure 45)

MOSFET and MESFET Devices Characterization

The mask includes large gated Hall devices and four smaller FETs (see Figure 48). All FETs have a $40\mu\text{m}$ gate width but different gate lengths of 4, 8, 24 and $36\mu\text{m}$.

The wafers yielded many good devices in both MESFET and MOSFET versions. Examples of the device I_D - V_{SD} vs V_g characteristics are shown in Figure 49.

The MESFET pinch off voltage was, as expected, about 10 volts (calculated based on $1\mu\text{m}$ epi doped to 10^{16}cm^{-3}). The low-field channel conductance vs gate voltage provided an estimate of the low field mobilities (I_S vs V_g^2) which gives μ of about $1000\text{cm}^2/\text{volt}/\text{sec}$ in film No. 32. This value compares well with the more accurate measurements performed on the gated Hall device where the source/drain channel extension does not enter into the calculation.

In the MOSFET devices the source/drain current is only partially modulated by the gate due to the fact that once the band bending reaches the inversion condition the channel is no longer affected by the gate potential and current saturation takes place. To fully cut off the channel current the epi thickness has to be reduced to about 3000\AA at the doping level of 10^{16} .

In general, the device characteristics were as expected and we thus successfully demonstrated the feasibility of fabricating devices on the multilayer films.

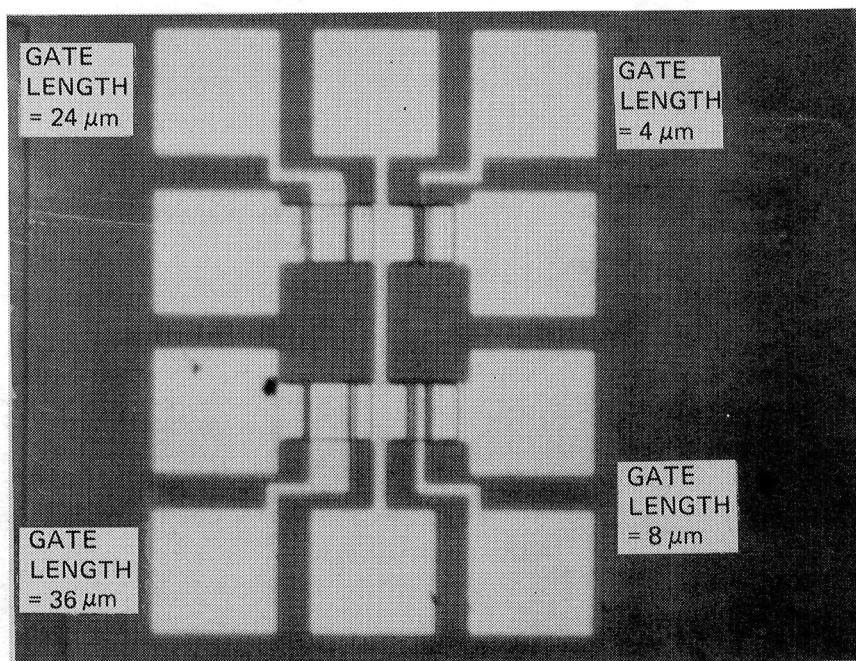
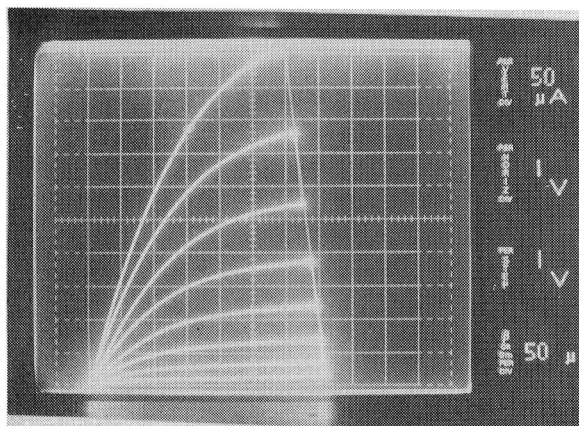
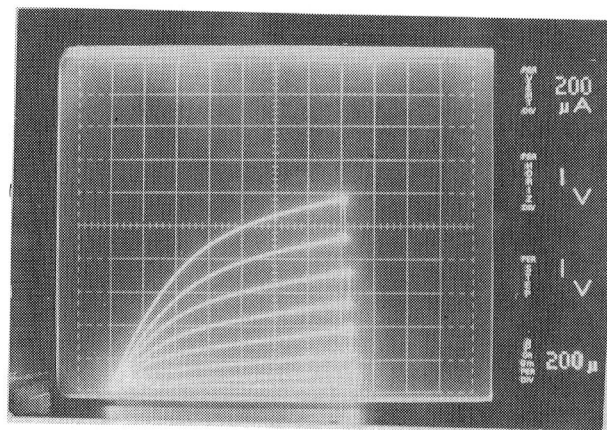


Figure 48. MESFET on $\text{Si}/\text{Si}_{1-x}\text{Ge}_x$ Film No. 324, Gate Width = $40\mu\text{m}$ Gate Lengths are X 36, 24, 8, and $4\mu\text{m}$

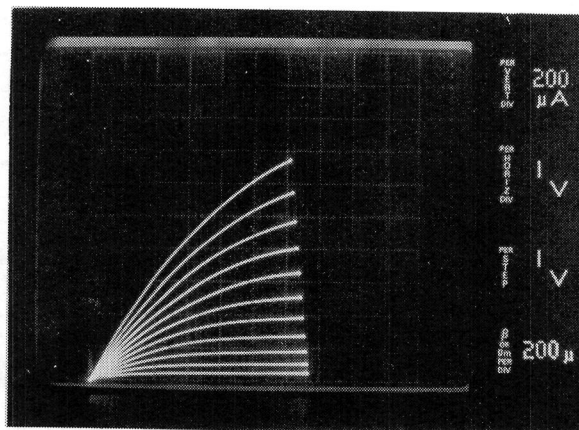


(a) No. 324



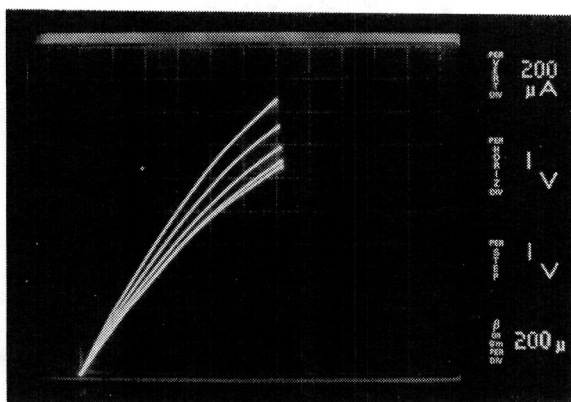
(b) No. 335

I_D - V_{SD} ; V_g FOR MESFET ON Si/SiGe

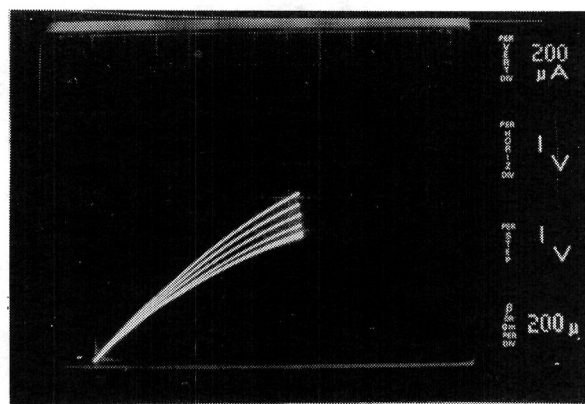


— C —

(c) I_D - V_{SD} ; V_g FOR MESFET ON Si No. 315



(d) DEVICE 314 (Si)



(e) DEVICE 342 (Si/SiGe)

Figure 49. I_D - V_{SD} ; V_g of MOSFET Devices

Summary

1. Thin silicon dioxide films were thermally grown on multilayer films using the uppermost Si layer. The oxide and its interface with the semiconductor (Si) seem to be the same as that on bulk Si.
2. Thermal oxide grown on multilayer films on which alloy layers are consumed shows no Ge content to within $\approx 1\%$ sensitivity. Ge pile-up at the oxide/semiconductor interface was detected.
3. MOSFET and MESFET devices were successfully fabricated on multilayer Si/SiGe films. Device performance characteristics were consistent with the measured multilayer film material parameters.

SECTION VI

DISCUSSION AND CONCLUSION

It is now worthwhile to summarize the most prominent features of the multilayer films.

1. Hall effect measurements of the films show the electron Hall mobility in multilayer films to be up to 50 percent higher than that of single layer of Si or SiGe alloy films of comparable total thickness and carrier density.
2. The enhanced mobility was observed for carrier density between 0.8×10^{16} and $2 \times 10^{17} \text{ cm}^{-3}$, in (100) oriented films but not on (111) films.
3. Carrier non-freezout occurs in the multilayer films at low temperature. Carrier density decreased by only a factor of 3 or 4 from 300°K to 20°K.
4. The mismatch in the lattice constants of the alloy and the Si layers is to a large extent accommodated in the multilayer films through elastic strain. The strain relief (e.g., through dislocations) in the multilayer and very thin films (e.g., 500Å) is considerably smaller than in thick alloy films (e.g., $>1 \text{ } \mu\text{m}$).
5. The electron density (n) and Hall and drift mobilities (μ^H, μ) are strongly modulated with depth, with the modulation period equal to the superlattice period. The peaks of n , μ^H , and μ almost coincide and occur at the SiGe on Si interfaces of the film. The modulation of n , μ^H , and μ increases sharply at lower temperature with the profile of n becoming δ -function-like at very low temperature.

The above experimental observations lead us to consider two distinctive mechanisms to account for the temperature dependence of the carrier distribution. The first is a dopant segregation model in which the dopant atoms are assumed to segregate to the interfaces during the film growth. This is assumed to happen as a result of gettering of the impurity atoms by the crystalline imperfections at the interfaces which are generated due to the mismatch between the two materials. The temperature dependence of the carrier profile can be accounted for as follows: At room temperature, thermal diffusion causes the broadening of the electron distribution with a characteristic length equal to the Debye length $D = 400\text{\AA}$ for $N = 10^{16}\text{cm}^{-3}$. At lower temperatures the electron distribution becomes less diffused and eventually at very low temperature it approaches that of the impurity distribution. The non-freezout is assumed to occur because the actual dopant concentration is much larger than the average value; possibly as high as 10^{18}cm^{-3} where the dopant activation energy is very small.

The second mechanism considered is electron transfer across the heterojunction due to the discontinuity (ΔE_c) in the conduction band as illustrated in Figure 50. Electrons transfer from the higher conduction band side to the lower conduction band side (assuming as in our case the two sides are n-doped). Band bending occurs due to the resultant electric field. With small ΔE_c , the electron distribution is fairly broad due to thermal diffusion but becomes sharper as the temperature is lowered. Carrier non-freezout should occur only if ΔE_c is larger than the activation energy of dopants in the higher conduction band side of the junction. The activation energy for phosphorus in Si is about 45 mV and thus the value of ΔE_c in the heterojunction should be larger than that to account for the non-freezout.

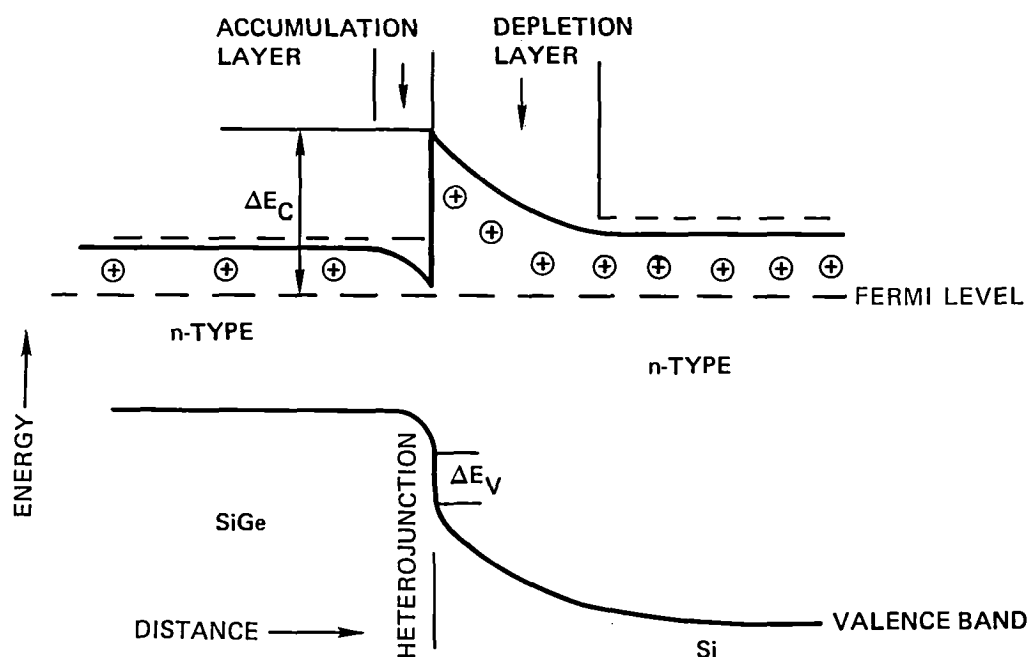


Figure 50. Ideal Energy Band Diagram of SiGe/Si Heterojunction

The question now is how do the two models account for the enhanced mobility and the mobility profile. In the dopant segregation model, the scattering due to ionized dopants in the bulk of the layers is expected to be less than that in an otherwise homogeneous semiconductor with the same average dopant density. This might result in higher average mobility, but the mobility should have its minimum value near the peak of N ; the reverse of what we saw in our films. In the electron transfer model, the separation of electrons from their parent dopant atoms should result in less scattering and thus higher mobility in the lower conduction band side of the heterojunction. This is consistent with the coincidence of the peaks of μ and n .

Remaining to be determined, however, is the electronic structure of the heterojunction between the Si and SiGe layers. An ideal heterojunction structure is shown in Figure 50. It is based on the assumption of the absence of interface states in the band gap. The value of ΔE_c (30mV) is obtained by assuming it is linearly proportional to the Ge content (~ 15 percent) and thus is equal to $0.15 \Delta E_c(\text{Si/Ge})$ where $\Delta E_c(\text{Si/Ge}) = .18\text{eV}$ is the conduction band discontinuity in the Si/Ge heterojunction (Ref 16). It should be noted that this value of $\Delta E_c(\text{Si/Ge})$ is deduced from the difference between the electron affinities of the two semiconductors and not from direct measurement.

The generation of interface states due to lattice imperfections can cause considerable complications in the electronic structure of the heterojunction. For example, in n-n heterojunctions the occurrence of acceptor type interface states in the band gap will result in an energy barrier at the heterojunction as shown in Figure 51 due to the formation of depletion layers on both sides of the junction. Other effects such as elastic strain can cause significant changes in the band structure. For example, the uniaxial strain in the (001) direction of 0.3 percent found in our films should result in the splitting of the lowest conduction band valleys - (001) relative to (100) and (010) - by about 25 meV determined from the deformation potential of Si which is $\sim 8.6\text{V}$ (Ref 17). The redistribution of electrons amongst these valleys is the major contributor to piezoresistance effect in n-type Si and Ge (Ref 18). Experimental determination of the electronic structure of the heterojunction is, however, necessary for better understanding of the problem.

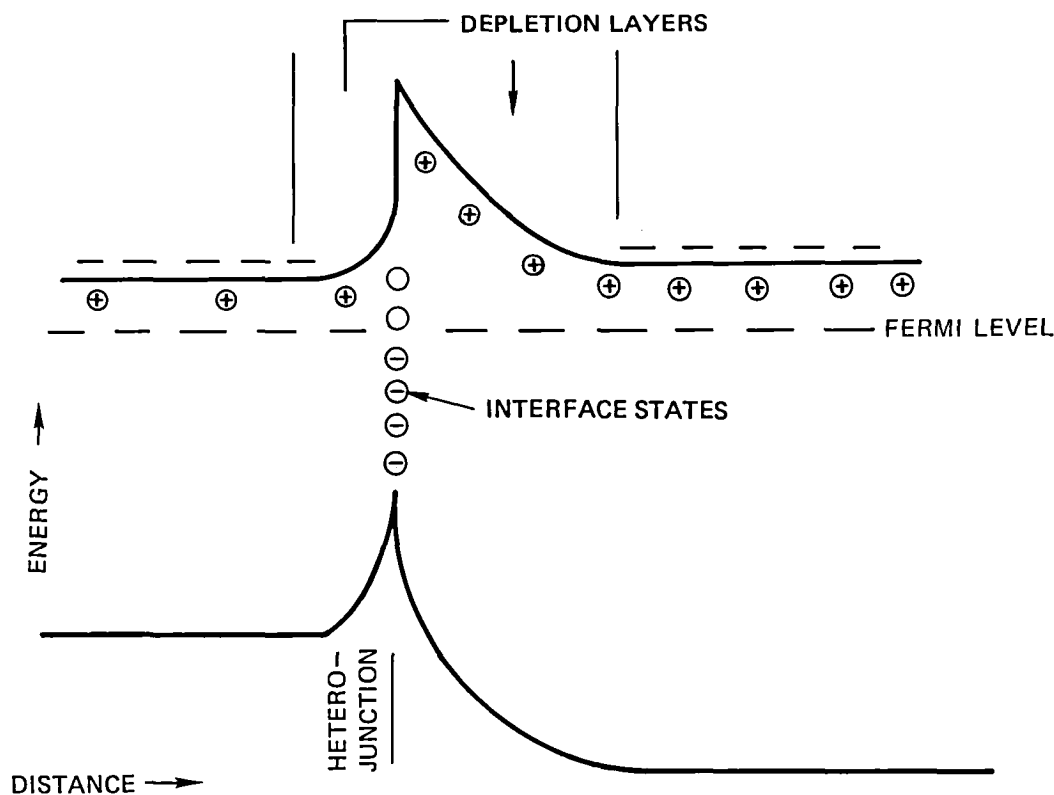


Figure 51. Energy Band Diagram of SiGe/Si Heterojunction with Interface States

Now, let us discuss the potential device application of the multilayer films. An important question is how high a mobility can be expected in these films. Mobility enhancement occurs due to several mechanisms including reduction of the scattering by separation of electrons from ionized dopants and piezoresistance effects due to tensile strain which causes the splitting of the conduction band valleys as mentioned above. Another related mechanism is the splitting of the conduction band valleys by the confinement of the electrons in narrow energy wells. This mechanism has been studied extensively in conjunction with the inversion layers in MOS devices (Ref 4, 17 and 19), and by Professor J. Moriarty of Cincinnati University in SiGe/Si superlattice (Ref 5). Electron confinement is known to occur in heterojunctions such as the GaAs/GaAlAs system and possibly occurs in our films. Unlike GaAs where the lowest valley of the conduction band is centered at the origin of the Brillouin zone, the Si valleys are located along the (100) direction and its equivalents. The quantization of the electron motion perpendicular to the plane of the film results in splitting of the energy bands into several sub-bands. The lowest sub-band corresponds to the (001) valley due to the fact that the largest effective mass is associated with that direction (see Figure 52). The energy difference between the sub-band and the next one is a function of the shape and depth of the well. If electrons occupy only the lowest sub-band, then their motion is two dimensional in nature and their effective mass is only $0.194 m_0$; the transverse mass of the ellipsoidal valleys of the Si conduction band. This is a factor of 1.4 smaller than the effective mass in bulk Si.

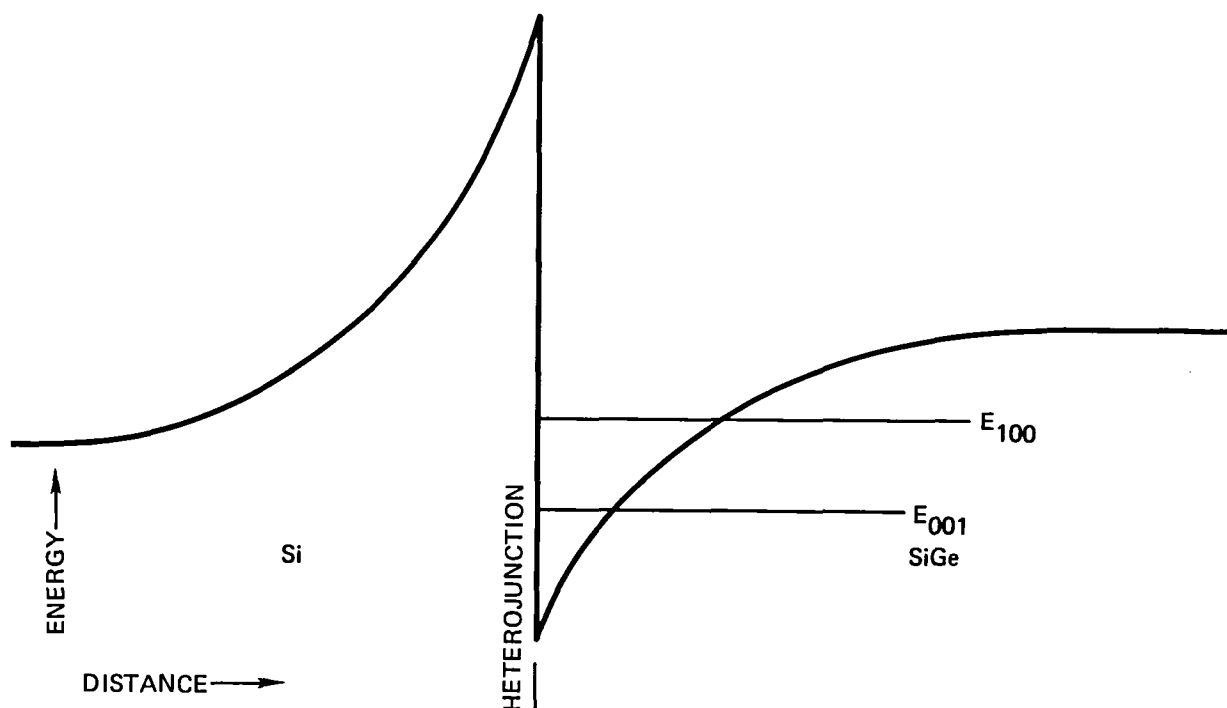


Figure 52. Hypothetical Energy Band Diagram of the Si/Si_{1-X}Ge_X Heterojunction

The first mechanism, namely, the separation of electrons from the ionized donors, brings the mobility to the value determined by phonon scattering, i.e., the mobility of lightly doped bulk semiconductor. For example, in the heterostructure of GaAs/GaAlAs the mobility obtained at room temperature is 8000 cm²/volt-sec which is the same as that of lightly doped GaAs. The mobility enhancement, however, is much larger at lower temperature where the ionized dopant scattering, usually the dominant mechanism at low temperature, is virtually absent. The electron mobility in lightly doped n-type Si is ~1500 cm²/volt-sec.

The second and third mechanism, the elastic strain (piezoresistance) and electron confinement both cause the splitting of the conduction band valleys. Their effect is additive only if the electron redistribution amongst the valleys is not complete. In the limiting case where electrons occupy only the lowest valley, the enhancement factor is 1.4; the ratio of the 2-d effective mass relative to the bulk effective mass. Thus, the expected electron mobility in an ideal heterostructure device, described in the next paragraph, can reach ~2,100 cm²/volt-sec. In bulk MESFET devices with carrier concentrations of ~10¹⁷cm⁻³ the mobility is about 800 cm²/volt-sec. In enhancement-type MOSFET devices the channel mobility is ~700 cm²/volt-sec.

An ideal film structure should be such that the lower band semiconductor — presumably SiGe — is undoped. The dopants should be incorporated in the higher band semiconductor preferably some distance away from the interface to minimize ionized impurity scattering. The thickness of the dopant layer should be such that it is completely depleted due to electron transfer across the heterojunction. Such film requirements might only be feasible in MBE grown films where low growth temperature minimizes dopant diffusion and where more precise control of layer thickness can be achieved. A set of film parameters suitable for use in MESFET devices is:

average carrier density $\sim 10^{17}$, total film thickness of about 2500Å, and layer thickness determined by the depletion requirement and ΔE_c . For $\Delta E_c \sim 50$ mV the optimum layer thickness is about ~ 2000 Å. The gate voltage required for fully depleting the channel is about 5 volts. Depletion type MOSFETS can be fabricated on films of similar parameters but of only about 1000Å thickness.

Suggestion for Future Studies

The experimental evidence obtained so far indicates strongly the occurrence of electron confinement at the heterojunctions. This mechanism can lead, as seen in the work of Moriarty (Ref 5) and others (Ref 4), to significant transverse mobility enhancement. It is thus of paramount importance to investigate the nature of this confinement. An immediate area of concern is the investigation of the electronic structure of the heterojunction between Si and SiGe layers. Another area is the transport properties at very low temperatures. For example, magnetoresistance experiments should be performed to search for Schubnikov-de Haas oscillation as evidence of electron confinement (2-dimensional electron gas).

SECTION VII

ABBREVIATIONS AND SYMBOLS

(100), (010), (001), (111) — Miller indices of crystal planes
Å — Angstrom units (10^{-10} Meters)
AES — Auger Electron Spectroscopy
Al — Aluminum
Au — Gold
B₂H₆ — Diborane
B_z — Magnetic field intensity in “depth” direction of gated Hall Device
C — Capacitance
CF₄ — Carbon tetrafluoride
ccpm — cubic centimeters per minute
cm — centimeters
cm⁻³ — per cubic centimeter
cm²/volt/sec — square centimeters per volt per second (unit of mobility)
CVD — Chemical Vapor Deposition
Cr — chromium
D — Debye length
E_x — Electrical field component along length of gated Hall device
E_y — Electrical field component along width of gated Hal device
EBMF — Electron Beam Micro-Fabricator
EDXS — Energy Dispersive X-ray Spectroscopy
FET — Field Effect Transistor
G — Channel conductance
GHD — Gated Hall Device
GaAs — Gallium arsenide
GaAlAs — Gallium aluminum arsenide
Ge — Germanium
GeH₄ — Germane
H₂ — Hydrogen
He — Helium
HCl — Hydrogen chloride
HF — Hydrogen fluoride

I — Electrical current
 I_D — Drain current
 J — Electrical current density
 K — Boltzmann constant
 $^{\circ}\text{K}$ — Degrees Kelvin
 KeV — thousand electron volts
 lpm — liters per minute
 L_x — Gated Hall device length
 L_y — Gated Hall device width
 LOCOS — “Local oxidation of silicon” method of electrical isolation
 m_0 — rest mass of electron
 mV — millivolts
 meV — milli electron volts
 mm — millimeter
 MBE — Molecular Beam Epitaxy
 MESFET — Metal-Semiconductor Field Effect Transistor
 MOSFET — Metal-Oxide-Semiconductor Field Effect Transistor
 MRDC — Microelectronics Research and Development Center
 MoSi_2 — Molybdenum silicide
 n — electron concentration density
 $n\text{-epi}$ — epitaxial layer with excess free electrons
 N_2 — Nitrogen
 N_A — Acceptor concentraton density
 N_D — Donor concentration density
 N^+ — Heavily doped N-tpe
 O_2 — Oxygen
 p — hole concentration density
 $p\text{-epi}$ — epitaxial layer with excess free holes
 ppm — parts per million
 P — Phosphorus
 pF — Picofarad
 PH_3 — Phosphine
 Pt — Platinum

PtSi_2 — Platinum silicide
 q — charge
RBS — Rutherford Backscattering Spectroscopy
 R_H — Hall Factor
rpm — revolutions per minute
S — Seconds
SEM — Scanning Electron Microscope
SIMS — Secondary Ion Mass spectrometry
Si — Silicon
SiGe — Silicon-germanium Alloy
Si/SiGe — Silicon on silicon-germanium alloy
SiC — Silicon carbide
SiGe/Si — Silicon-germanium alloy on silicon
 SiH_2Cl_2 — Dichlorosilane
 SiH_4 — Silane
 SiO_2 — Silicon dioxide
T — Temperature (degrees Kelvin)
TEM — Transmission Electron Microscopy
V — Volts
 V_{SD} — Source-drain voltage
 V_g — Gate voltage
W — Depletion width of gated Hall device
 u — mobility
 u_H — Hall mobility
 μm — microns or micrometers (10^{-6} meters)
 $\left. \begin{array}{l} x \text{ — length} \\ y \text{ — width} \\ z \text{ — depth} \end{array} \right\}$ directions on gated hall device

SECTION VIII

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16. Abstract <p>This report describes the investigation of the growth, properties, and the structure of epitaxial multilayer Si/Si_{1-x}Ge_x films grown on bulk Silicon Substrates. It also describes the fabrication and characterization of MOSFET and MESFET devices made on these epitaxial films.</p> <p>Films were grown in a CVD reactor using hydrides of Si and Ge with H₂ and He as carrier gases. Growth temperatures were between 900°C and 1050°C with most films grown at 1000°C. Layer thickness was between 300Å and 2000Å and total film thickness was between 0.25µm and 7µm. The Ge content (X) in the alloy layers was between .05 and 0.2.</p> <p>N-type multilayer films grown on (100) p-type Si showed Hall mobility in the range 1000 to 1500 cm²/Vsec for an average carrier concentration of ~ 1 x 10¹⁶ cm⁻³. This is up to 50% higher than the Hall mobility observed in epitaxial Si films grown under the same conditions and with the same average carrier concentration. The mobility enhancement occurred in films with average carrier concentration (n) from 0.7 x 10¹⁶ to 2 x 10¹⁷ cm⁻³, and total film thickness greater than 1.0µm. No mobility enhancement was seen in n-type multilayer films grown on (111) Si or in p-type multilayer films.</p> <p>The structure of the films was investigated using SEM, TEM, AES, SIMS, and X-ray double crystal diffraction techniques. The film composition profile (AES, SIMS) showed that the transition region between layers is of the order of about 100Å. The TEM examination revealed a well defined layered structure with fairly sharp interfaces and good crystalline quality. It also showed that the first few layers of the film (closest to the substrate) are uneven, most probably due to the initial growth pattern of the epitaxial film where growth occurs first in isolated islands that eventually grow and coalesce. The X-ray diffraction measurement determined the elastic strain and strain relief in the alloy layers of the film and the elastic strain in the intervening Si layers. The strain relief in thick alloy layers was found to be considerably larger than that in thin alloy layers, indicating that the mismatch between the lattice parameters of the alloy and Si is accommodated mostly by elastic strain in thin layers. The elastic strain in the Si_{1-x}Ge_x and the Si layers are -0.3% and + .2% respectively. Measurement of the carrier density and Hall Mobility as a function of temperature showed that the carriers do not completely freeze-out at very low temperatures (≤50°K). The measurement of the carrier concentration profile (C-V measurement) within the film showed very strong periodic variation of with depth. The peaks of n are coincident with the SiGe-on-Si interfaces. Hall and drift mobility profiles were also strongly modulated with their peaks almost coincident with those of n. The modulation of n and the mobility increase with decreasing temperature.</p> <p>The above results indicate electron confinement might be occurring at the layer interfaces of the multilayer films. The mechanism of electron confinement is not clear at this time. Factors that probably play important roles are the conduction band discontinuity at the heterojunction and the elastic strain in the SiGe and Si layers.</p>					
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